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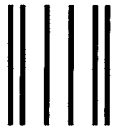

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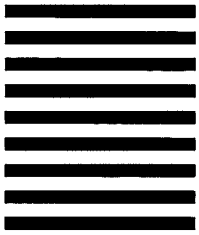

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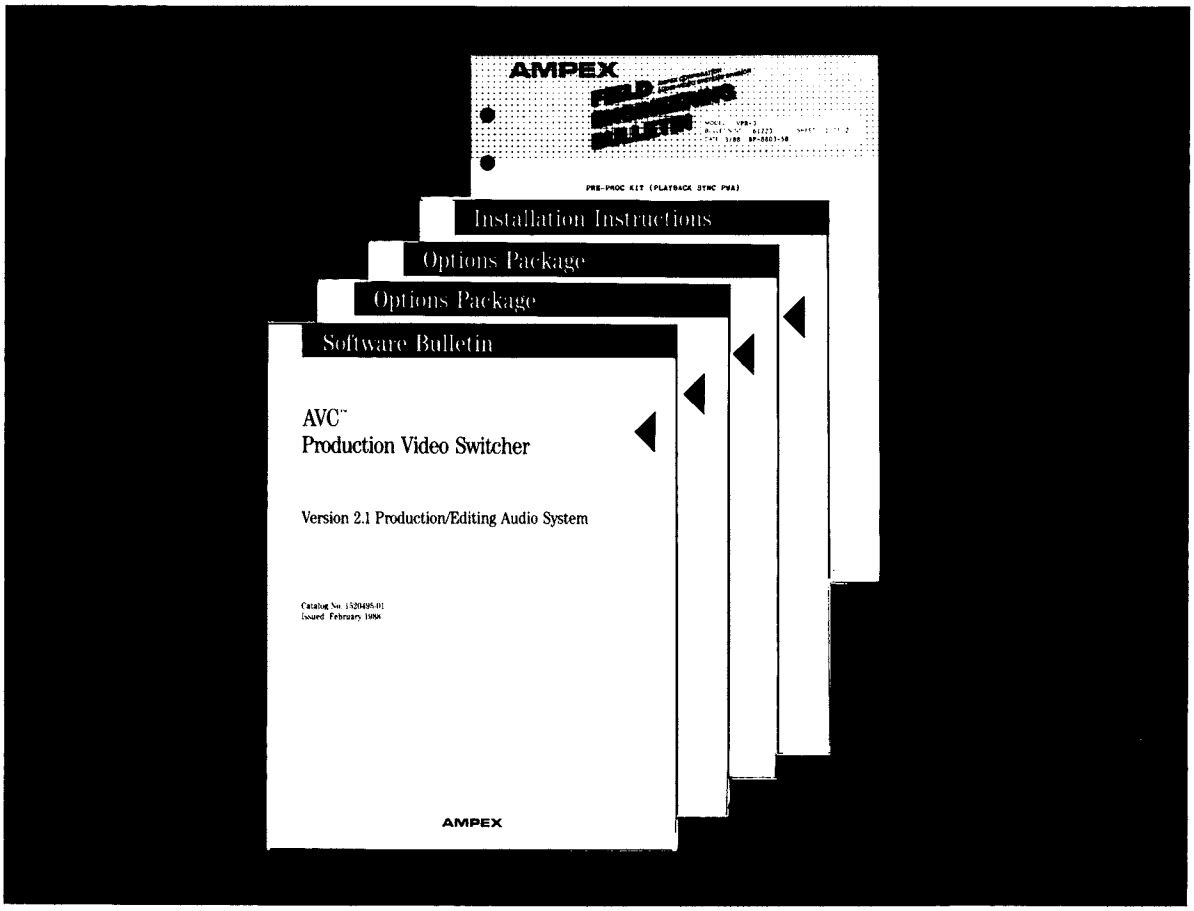

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AMPEX CORPORATION
401 BROADWAY
REDWOOD CITY, CALIFORNIA 94063
(415) 367-2011

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International

AUSTRALIA
Ampex Australia Pty. Ltd.
P.O. Box 199
55-61 Talavera Road, Unit A
North Ryde, 2113
New South Wales, Australia

21 Terra-Cotta Drive
Blackburn
Victoria, Australia

BELGIUM
Ampex S.A. Nivelles
Rue du Progres 10
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BRAZIL
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Avenida Portugal 54
Urca CEP 22291
Rio de Janeiro, RJ Brazil

CANADA
Ampex Canada Inc.
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L5N 3S7, Canada

1116-55 Avenue, N.E.
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T2E 6Y4, Canada

729 Meloche Street
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Bogota, Colombia

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Acre Road, Reading
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GERMANY
Ampex Europa GmbH
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West Germany

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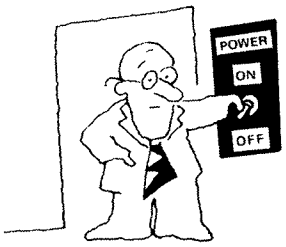
Safety and First Aid Suggestions

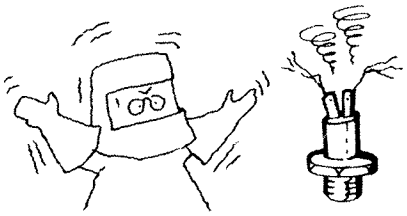
Regardless of how well electrical equipment is designed, personnel can be exposed to **dangerous electrical shock** when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of the first aid related to electrical hazards.

In addition, the following safety practices must be followed:

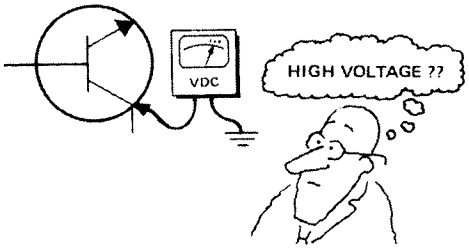


Do not attempt to adjust unprotected circuit controls or to dress leads with power **on.**

Always avoid placing parts of the body in series between ground and circuit points



To avoid burns, do not touch heavily loaded or overheated components without precaution.



Remember that some semiconductor cases and solid-state circuits carry high voltages.

Do not asssume that all danger of electrical shock is removed when power is **off.** Charged capacitors can retain dangerous voltages for a long time after power is turned off. These capacitors should be discharged through a suitable resistor before any circuit points are touched.

Don't take chances. Be fully trained. Ampex equipment should be operated and maintained by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, **turn power off** before rendering aid. Muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

WARNING

DO NOT TOUCH VICTIM OR HIS CLOTHING BEFORE POWER IS DISCONNECTED OR YOU CAN ALSO BECOME A SHOCK VICTIM.

If power cannot be turned off immediately, **very carefully** loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

Good Practices

In maintaining the equipment covered in this manual, please keep in mind the following, standard good practices:

When connecting any instrument (oscilloscope, waveform, monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminally internally.

When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.

When troubleshooting, remember that FETs and other metal-oxide semiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.

When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.

When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.

Warning

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case, the user, at his own expense, will be required to take whatever measures may be necessary to correct the interference.

Note

This system was tested using the shielded interconnect cables provided with the unit. Failure to use the cables provided may result in radio interference outside acceptable limits.

Notice

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus as set out in the Radio Interference Regulations of the Canadian Department of Communications.

Cet appareil digital n'excède pas aux normes classe A pour bruits radioélectriques des appareils digitals dans le Règlements sur le Brouillage Radioélectriques du Bureau de Communications du Canada

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SECTION 1

GENERAL INFORMATION

1-1 SCOPE OF MANUAL

This manual provides general information, operating theory, and maintenance and service information for the ACE 25 Computerized Editing System. The ACE 25 system is shown in Figure 1-1, and a typical studio configuration is shown in Figure 1-2.

The material covered in this manual is presented as follows:

- Section 1 contains an overall description of the system, including information on system options and peripheral equipment, television standards and formats, audio formats, and Ampex maintenance policy.
- Section 2 presents the system theory of operation.
- Section 3 covers system maintenance, troubleshooting procedures, and diagnostics.
- Section 4 describes replacement of assemblies.
- Sections 5 through 16 cover the theory of operation and adjustment and repair for PWAs and system components.
- Appendices A through F provide information on error messages, conversion among different television standards, EDL transfer using RS-232 communications, VPR-2/VPR-2B interface modification, and ACE MIF (Machine Interface) installation.

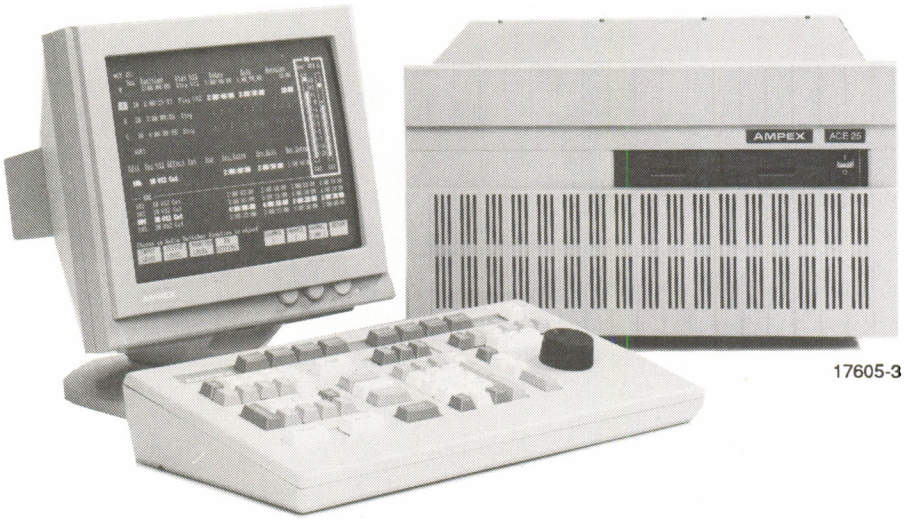


Figure 1-1. ACE 25 Computerized Editing System

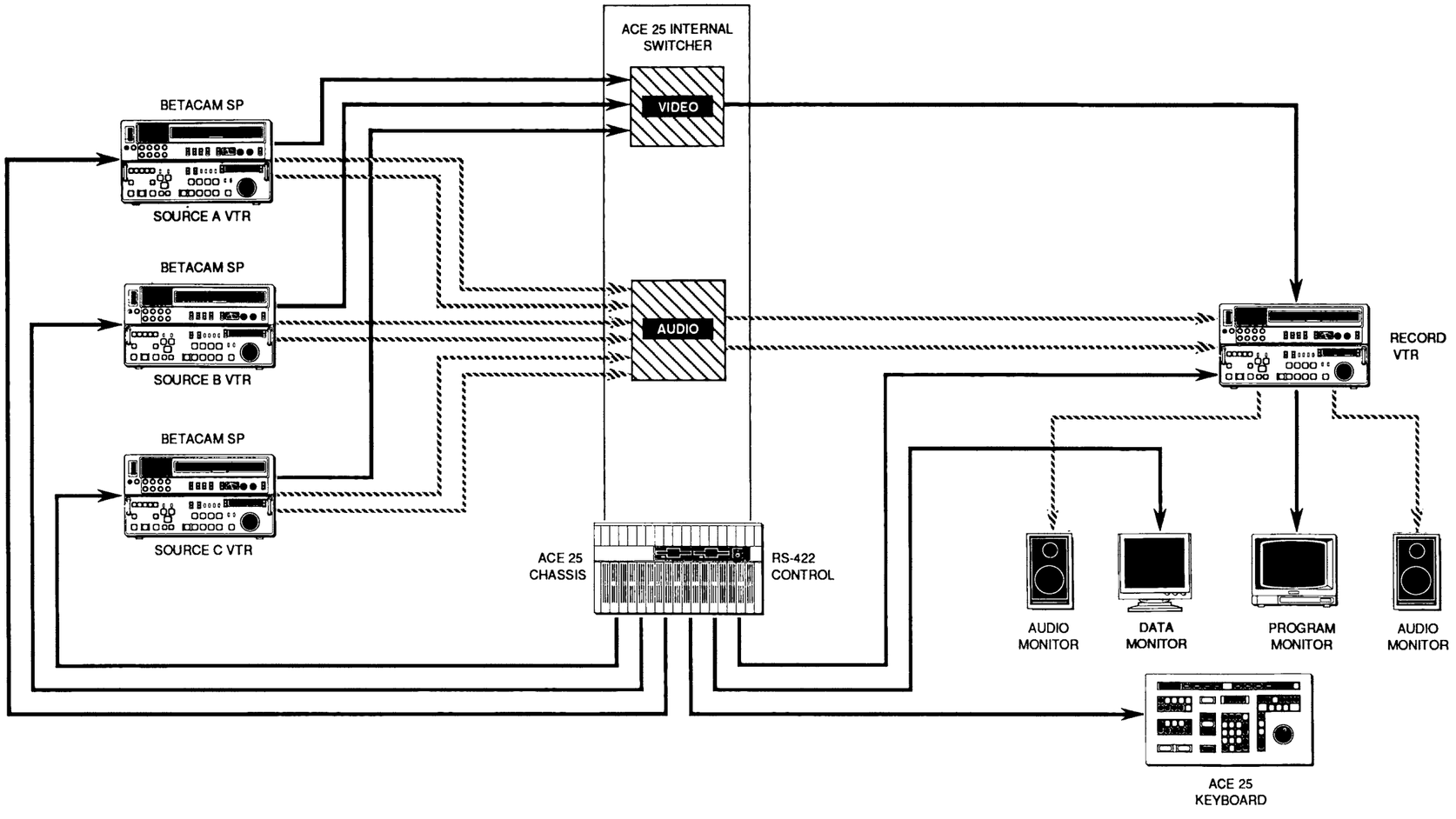


Figure 1-2.
Typical Editing System Configuration

1-2 CAPABILITIES

ACE 25 is a computer-based editor which can control up to 4 VTRs (3 source and 1 record), 4 external GPI device outputs, and an audio and a video switcher. ACE 25 is available in the NTSC, PAL, or PAL-M television formats, and operates with optional internal or external audio and video switchers.

In one simple system, ACE 25 provides a 4-machine editor, 6-input audio mixer, 6-input video switcher, audio EQ control, and on-screen audio metering. The ACE 25 is a full-function editor that can be used for a wide range of editing tasks. Edit decision lists and operator parameters can be stored on disk for future use.

The ACE 25 system gives the editor a choice of cuts, keys, dissolves, and other special effects, allowing input of in/out edit points, pre-roll and post-roll values, dissolves and effect durations, and other parameters.

The system is software-controlled, offering great flexibility and operational ease. During an edit session, each edit decision is compiled automatically into an edit decision list (EDL). Edits in EDLs can be modified to incorporate changes before being committed to tape, then saved on floppy disk (3.5-inch), or transferred to a printer.

Tape machines compatible with the ACE 25 system include the VPR-300 (D-2 format), 1-inch helical VTRs (such as the VPR-2/VPR-2B, VPR-3, VPR-6, or VPR-80), CVR-series Betacam and Betacam-SP VCRs, U-Matic VCRs, and M-II VCRs. External switcher interfaces include the Penguin (Dedicated Editing Switcher), Vista Production Switcher, and the Grass Valley Group GVG-100. Some of the tape machines listed above require internal modifications and Ampex machine interface units (MIFs). For more information, refer to Appendix A, "Installation," of the *ACE 25 Computerized Editing System Operation* Manual.

Available options for the ACE 25 system include a rack mount monitor, a comments keyboard, a composite data video kit, and internal audio and video switchers.

1-3 PHYSICAL DESCRIPTION

The basic ACE 25 system consists of three units: a rack-mountable chassis unit (Edit Controller), a small desktop keyboard, and a desktop monochrome monitor. Optional internal switchers or external switchers are available.

1-4 Edit Controller

The Edit Controller is the center of the system. It is enclosed in a 10.5-inch high rack-mountable chassis. The Edit Controller contains an 80286 microprocessor-based CPU (AT-type) with one megabyte of memory (RAM), two 3.5-inch floppy disk drives, a floppy disk controller PWA, a Monochrome Display Adaptor PWA, an 8-Channel Intelligent Line Controller (ILC) PWA, a Color Framer/GPI PWA and a Regulator PWA, plus a power supply and cooling fan. The Edit Controller may also contain a Switcher Backplane PWA with an optional audio and/or video internal switcher and a Rear Panel I/O PWA may also be present to support rear panel connections.

Figure 1-3 shows an interior view of the Edit Controller, and Table 1-1 lists the PWAs in the Edit Controller. Figure 1-4 shows the rear panel connections.

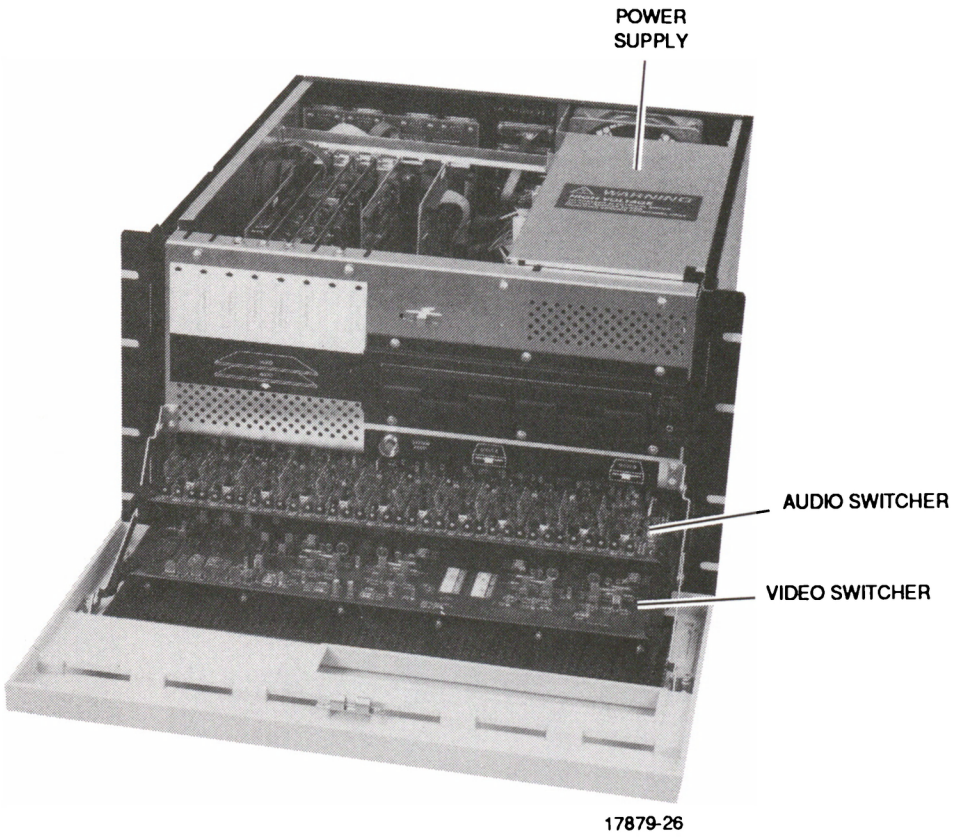
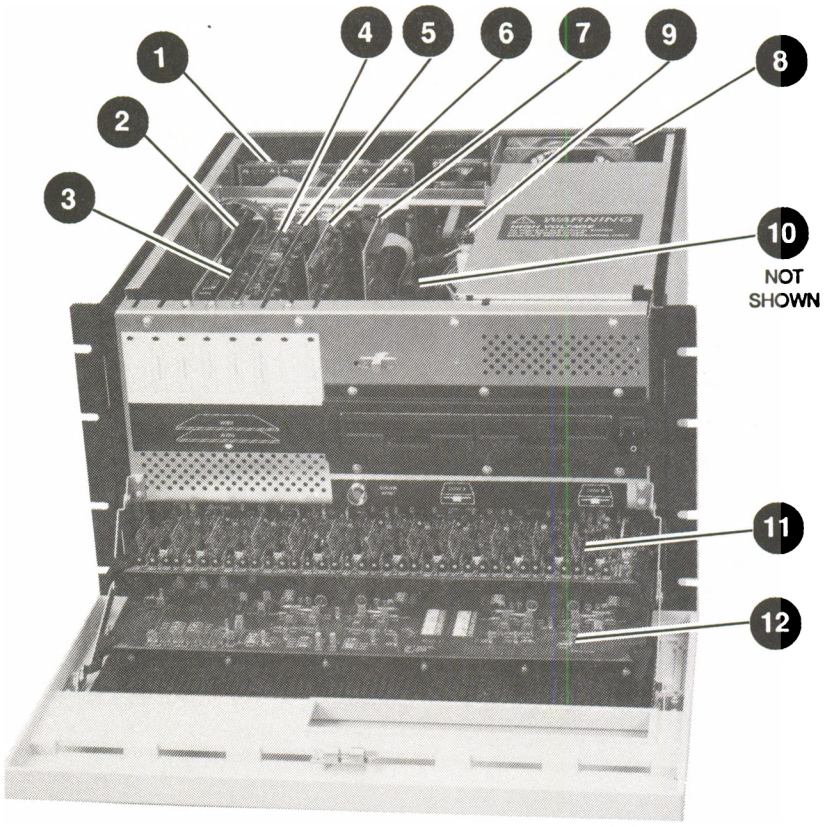


Figure 1-3. Edit Controller Unit

Table 1-1. Edit Controller PWAs



Index	PWA	Function
1	Input/Output Panel PWA	Contains external input/output interface connections
2	Dumpster Bus Interface PWA	Interfaces Switcher PWAs to Dumpster Bus
3	Video Timing PWA	Controls internal video timing
4	Color Field 1 Detector PWA	Sets color framing
5	8-Channel ILC PWA	Controls RS-422 devices; contains battery-backed RAM

(Continued next page)

Table 1-1. Edit Controller PWAs (Continued)

Index	PWA	Function
6	Data Video Display PWA	Controls Display Monitor
7	Disk Drive Controller PWA	Controls Disk Driver input/output
8	Switcher Backplane PWA (not shown)	Interfaces internal switchers with system
9	Regulator PWA	Regulates Power Supply
10	CPU Motherboard PWA	Runs main program
11	Composite (or Component) Video Switcher PWA	Switches video signals
12	Audio Switcher PWA	Switches audio signals

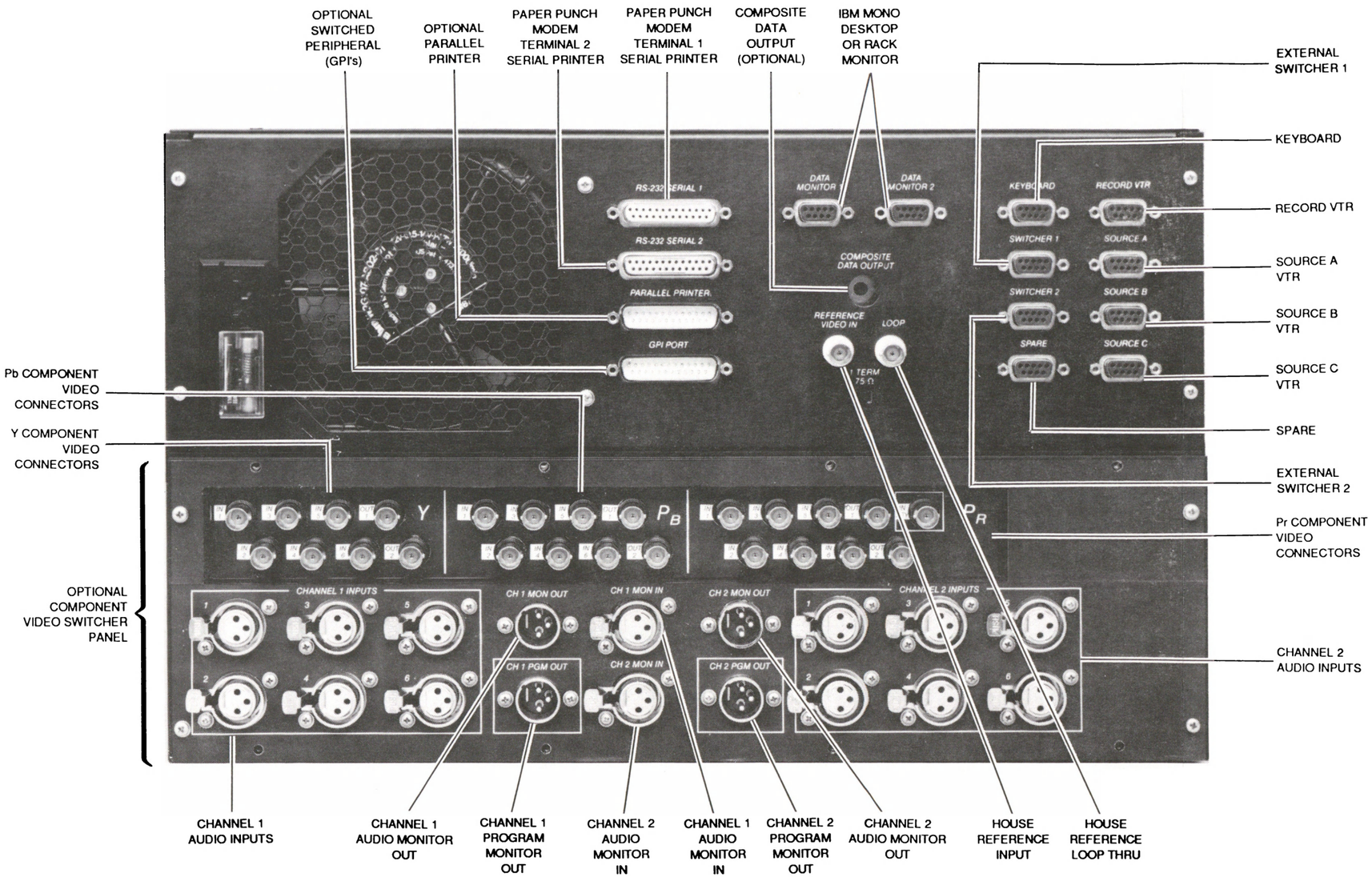


Figure 1-4.
Edit Controller Rear Panel

1-5 Keyboard Unit

The keyboard unit, shown in Figure 1-5, is connected to the Edit Controller by a cable with a 9-pin "D"-type connector, and is used by the operator to input commands and data to the ACE 25. An optional comments keyboard can be attached to the keyboard (any IBM AT-compatible keyboard with 5-pin DIN connector). For a description of the keyboard keys, refer to the *ACE 25 Computerized Editing System Operation* Manual.

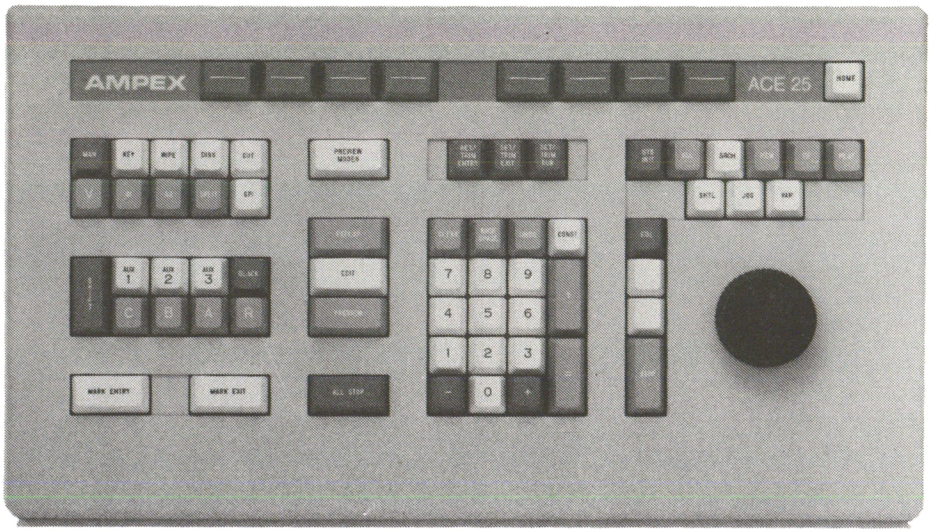


Figure 1-5. ACE 25 Keyboard Unit

1-6 Data Monitor

A tabletop data monitor is typically used with the ACE 25 system. Figure 1-6 shows the data monitor and identifies the location of monitor controls. The data monitor is connected to the rear panel of the Edit Controller. An optional rack-mount monitor may be used in addition to, or in place of, the tabletop data monitor.

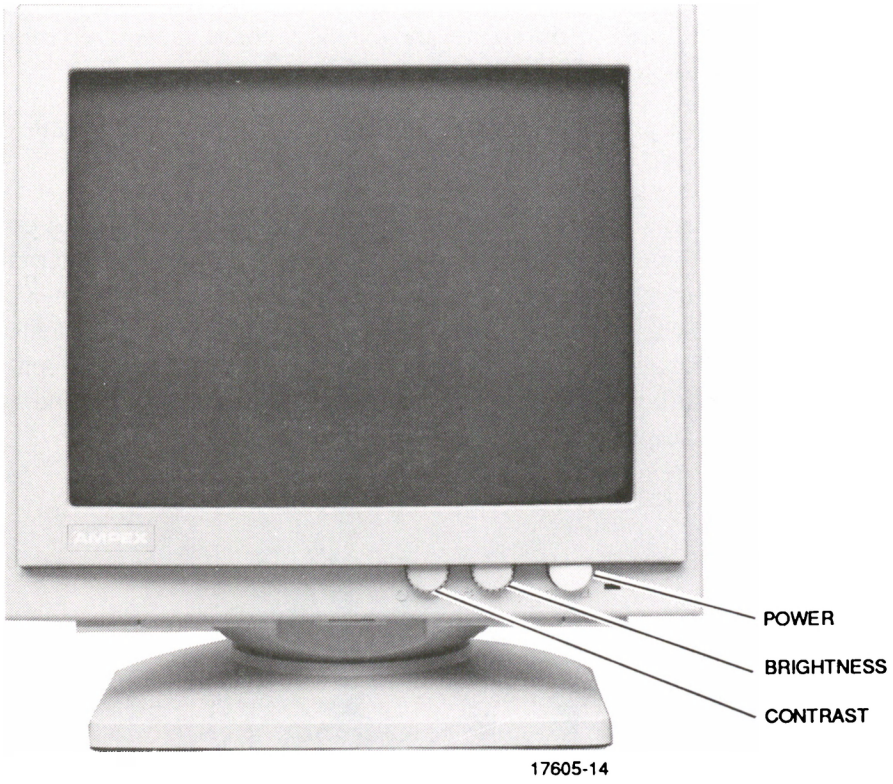


Figure 1-6. Tabletop Data Monitor

1-7 Optional Internal Switchers

Located below the editing electronics in the edit controller chassis are two slots for optional internal switchers. If internal switchers were ordered with the system, the boards will already be installed. They can be installed later by a field service engineer or studio engineer with guidance from Ampex.

The full internal switcher complement includes a single board audio switcher and a single board video switcher in either composite or component formats. A switcher interface kit, which includes rear-chassis I/O (input/output) panel and extender board, is required for internal switcher operation. The switcher interface kit can be factory or field installed.

Internal switcher control is assigned via software in ACE 25's system initialization menus. Switcher crosspoints are also assigned in the initialization menus.

The ACE 25 optional internal audio switcher is shown in Figure 1-7. This PWA can control six external audio sources (three source VTRs and three auxiliary sources), an internal tone generator, and silence. Two channels for each external audio source are supported on a basic A/B bus mix system. The audio switcher controls cuts, dissolves and three bands of equalization with full split audio capability. The audio signals and EQ settings are brought to the menu monitor and displayed via high-resolution VU meters and bar-graphs. The ACE 25's transport control knob is used to set input levels, output levels, monitor levels, and EQ settings.

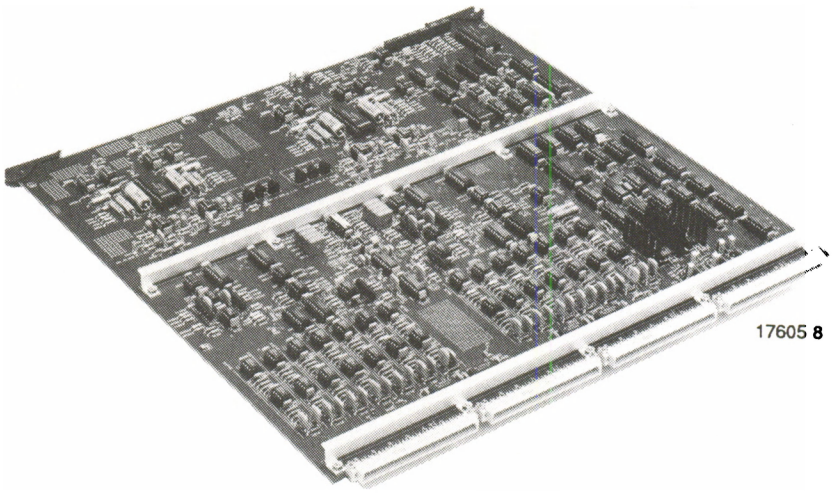


Figure 1-7. Internal Audio Switcher

The ACE 25 optional internal component video switcher is shown in Figure 1-8. This switcher can control up to six sources of external component video (three source VTRs and three auxiliary sources), and video black. The component video switcher controls cuts, dissolves, full split video capability, and a single key channel in a basic A/B bus mix system. The component switcher can also perform component chroma keys. The ACE 25's shuttle knob is the only control required to set manual fader position, A/B bus video mix levels, key clip levels, key gain levels, and component chroma key hue settings.

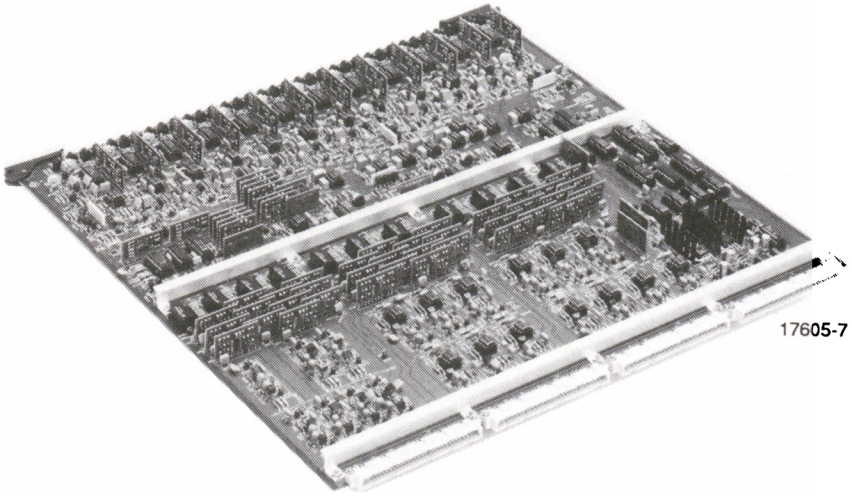


Figure 1-8. Internal Component Video Switcher

The ACE 25 optional internal composite video switcher is shown in Figure 1-9. This switcher controls six external composite video sources (three source VTRs and three auxiliary sources), and an internally-generated video black. The composite video switcher controls cuts, dissolves, full split video capability, and a single key channel in a basic A/B bus mix system. The ACE 25's shuttle knob is the only control required to set manual fader position, A/B bus video mix levels, key clip levels, and key gain levels.

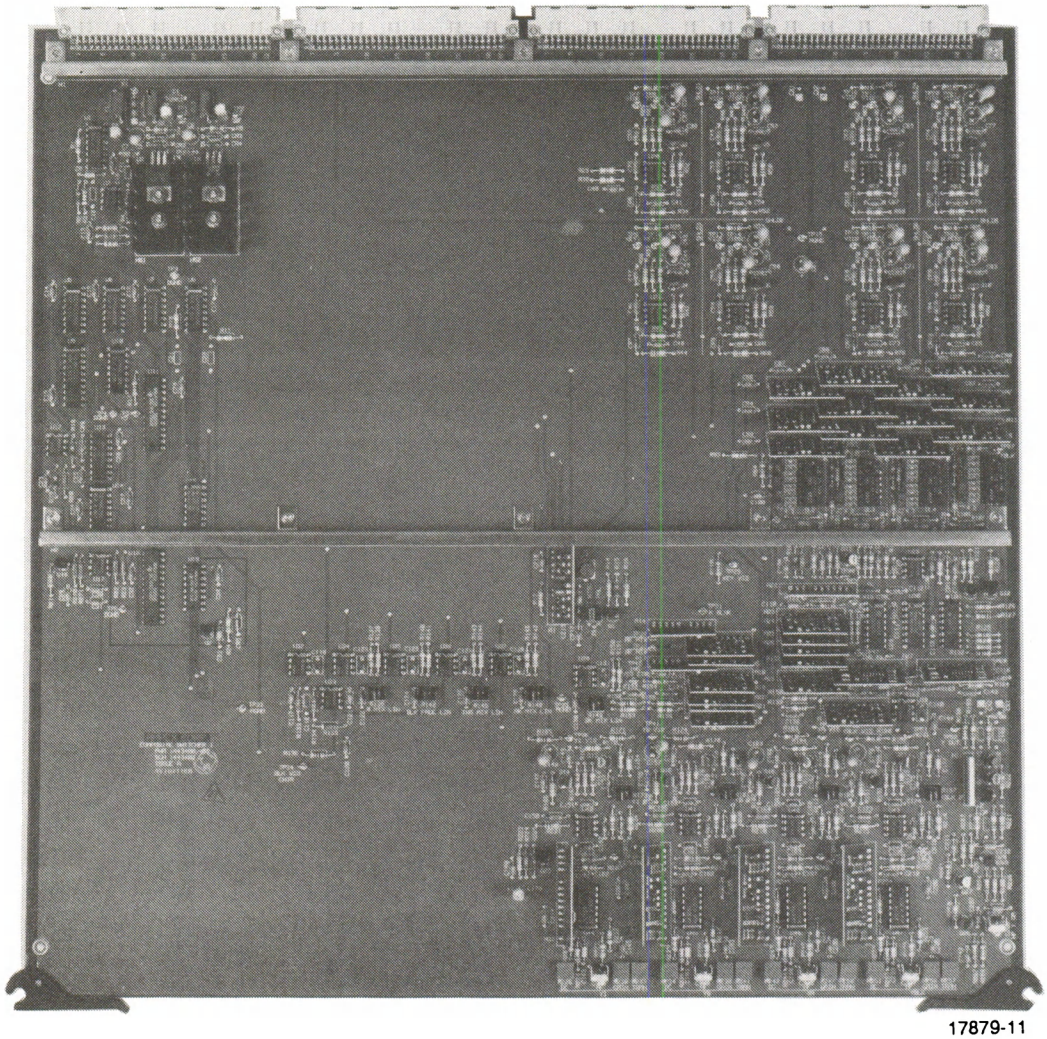


Figure 1-9. Internal Composite Video Switcher

1-8 Optional External Switchers

The ACE 25 can use a number of external switchers, including:

- Dedicated Editing System
- Vista Production Switcher
- Grass Valley Group GVG-100

1-9 SOFTWARE DESCRIPTION

The ACE 25 is a software-based editing system, with user-defined parameters for machine control and editing functions. ACE 25 software consists of an operating system (based on MS-DOS) , a set of user programs, a common data base, and power-up diagnostics. At system startup, software is loaded from the ACE 25 system disk into the Edit Controller main memory and the ILC memory.

The operator interface with the ACE 25 software consists of operator input through the keyboard and transport control knob, and system output through a monochrome display monitor. The system interprets and processes key codes from the keyboard, and checks the transport control knob position and movement direction during certain operations, such as VTR control.

ACE 25 uses the MS-DOS operating system as a slave to perform basic I/O functions for the disk drives, printer, RS-232 ports, comments keyboard port, and system clock. All interaction with the MS-DOS operating system is through a single pSOS process which executes normal DOS system calls.

The ACE 25 communicates with the video and audio recorders and players, plus any external switchers, via RS-422 serial lines. ACE 25 sends commands to these devices, which then reply to ACE 25. The communications protocol and data formats vary depending on the device. ACE 25 uses a dc pulse trigger to the GPI ports, to trigger outside events based on timing specified by the operator. The timing board in the ACE 25 provides a video field rate interrupt to the software. A status port provides color framing information along with a counter, which gives the current position within a video field.

1-10 EDL FORMAT

ACE 25 stores EDL (edit decision list) files on disk, in either CMX or SMPTE format . A unique internal format of the EDL is used within ACE 25, as described below.

An EDL is kept as a double-linked list of edits. A list structure gives the top and bottom of each edit decision list, along with its title. Each list is referenced through a set of data values called a list viewport. The list viewport consists of a pointer to the list, a pointer to the current edit, the current line number in the edit, and a comment cursor offset.

Each edit in the list consists of a fixed size header, with associated line blocks. The header contains:

- Edit size (in bytes)
- Segment number of next edit
- Segment number of previous edit
- Edit number (SMPTE-compatible, 6 digits plus letter)
- Edit status flags
- Audio output level

Each line block contains the line block size, the type of line block, and then the body of the block. The line block types include: COMMENT, TRIGGER, CUT and EFFECT. The body of each line block is a structure with fields for each of the appropriate edit parameters.

Whenever a request is made which could modify an edit, the edit is first copied into a change buffer, where modifications are made. When the request is complete, the change buffer is then compared with the original edit. If the modified edit is the same as the original edit, noting happens. If the modified edit is different than the original edit, the original edit is copied into a storage area called the Undo buffer then replaced with the modified edit.

A copy of the EDL is stored in battery-backed RAM on the Color Field 1 Identifier PWA, to ensure EDL integrity during power outages. New or modified edits are linked into the EDL before the old edit is removed.

1-11 TELEVISION STANDARDS AND FORMATS

The ACE 25 can be configured for these television standards:

- NTSC (525 lines, 60 Hz)
- PAL (625 lines, 50 Hz)
- PAL-M (625 lines, 60 Hz)

The optional internal component video switcher can be configured to process component video signals in one of the following formats:

- SMPTE Component
- EBU Component
- PAL-M Component

The optional internal composite video switcher can be configured to process composite video signals in one of the following formats:

- NTSC
- PAL
- PAL-M

Appendix B describes conversion procedures for the different television standards.

1-12 AUDIO FORMATS

The ACE 25 is designed to edit standard analog audio sources. The optional internal audio switcher can control up to eight analog audio sources, with two channels per source. Standard XLR connectors are used for input and output connections. When Betacam SP VCRs are used with the ACE 25, only audio on channel 1 and channel 2 can be used.

1-13 MAINTENANCE POLICY

The following paragraphs summarize warranty coverage for the ACE 25, and Ampex policy regarding maintenance and technical support. Ampex customer support plans are also discussed.

1-14 Warranty

Warranty coverage is described in the Terms and Conditions of Sale agreement, an integral part of every Ampex sales contract. Unless specific exceptions are noted on the contract, Ampex warrants to the original purchaser that the ACE 25 system will be free from defects in material and workmanship for one year from date of shipment by Ampex. Refer to the Terms and Conditions of Sale agreement to determine warranty coverage in effect at time of purchase.

1-15 Technical Support

If the customer experiences technical difficulty with the ACE 25 system, service and assistance are available at the nearest Ampex regional office, whether or not the warranty period has expired. A list of offices appears on page iv at the front of this manual. Do not return parts to the Ampex factory or service center without prior written authorization from Ampex. All communication with Ampex technical support services should be made through the regional sales offices.

1-16 Repair

Repairs can entail replacement of entire subassemblies, PWAs, or component parts. If the ACE 25 system is under warranty, repairs can be requested through a regional sales office, under a parts exchange program. Whether or not the ACE 25 is under warranty, the degree of convenience with which repairs are made depends on the Ampex support plan selected by the customer.

1-17 Support Plans

Ampex makes available a variety of support plans to its customers. Each plan includes a spare parts kit that can be composed of entire subassemblies, PWAs, or component parts, such as integrated circuits. The range of customer support plans is flexible, and a plan can be tailored to individual operational requirements and budget considerations. Contact the appropriate sales office for details.

1-18 CONVENTIONS

This manual adopts the following conventions:

- The ACE 25 is also called the system, or the editing system.
- The CPU Motherboard PWA is also called the system board.
- Transports refer to either video tape transports or audio tape transports, unless one type is specified.
- Hard keys (dedicated keys on the ACE 25 keyboard with legends identifying their functions) are indicated in **BOLD CAPITALS.**
- Soft keys (eight keys at the top of the keyboard, without legends, whose functions are displayed at bottom of display screen) are indicated in ***BOLD ITALIC CAPITALS.***
- Software identifiers and signal names appear in CAPITALS and are frequently abbreviated.

1-19 RELATED PUBLICATIONS

The following publications provide additional information on the ACE 25:

- *ACE 25 Computerized Editing System Operation,* Catalog No. 1520498
- *ACE 25 Parts Lists and Schematics,* Catalog No. 1520500
- *Dedicated Editing Switcher Service Manual,* Catalog No. 1809531

This manual contains information which originally came from vendor-supplied manuals. Information on IBM AT-compatible computer systems can be found in numerous non-Ampex publications.

SECTION 2

SYSTEM THEORY OF OPERATION

2-1 INTRODUCTION

This section describes system theory of operation for the ACE 25 system, including control and audio/video signal flow, and an overview of ACE 25 software. Sections 6 through 16 include information on the operation of each major sub-assembly or PWA in the ACE 25 system.

2-2 OVERALL BLOCK DIAGRAM

An overall block diagram of the ACE 25 system is shown in Figure 2-1. The Edit Controller unit contains the CPU Motherboard PWA with the PC AT Input/Output bus, the optional video and audio internal switchers, the Dumpster Bus Interface PWA, the Video Timing Generator PWA, the Color Field 1 Identifier PWA, the 8-Channel ILC PWA, the Data Video Display PWA, the Floppy Disk Drive Controller with the disk drives, and power supply with Regulator PWA and a Reset switch. The Input/Output Panel interfaces external devices to the Edit Controller.

The CPU Motherboard with its I/O bus is the central part of the ACE 25 system. Power is supplied from the Regulator PWA and power supply. The Floppy Disk Drive Controller PWA handles data transfer between the CPU and disk drives. The Data Video Display PWA is linked to the Data Monitor Driver in the Input/Output Panel, which can drive two display monitors.

The 8-Channel ILC PWA is connected to the Input/Output Panel for SMPTE ES Bus (RS-422) communications. One channel is used for interfacing with the ACE 25 keyboard. Another channel is reserved for an auxiliary device. Two channels are reserved for interfacing with external switchers. The remaining four channels are connected to VTRs or ATRs (one record and three source machines).

Reference video is looped through the I/O Panel, and sent to the Color Field 1 Identifier PWA for internal use, then passed to the Video Timing Generator PWA. The Color Field 1 Identifier PWA (also called the Color Framer PWA) handles the GPI ports, and stores the EDL in battery-backed memory. This PWA is also linked to the internal switchers.

The Video Timing PWA provides timing signals to the Dumpster Interface PWA, which passes the signals to the switchers.

The Dumpster Bus Interface PWA transfers switcher control and timing information to the internal audio and video switchers through the switcher backplane. The record and source video signal lines are linked to the switcher backplane through connectors on the rear panel.

Two RS-232 ports and a printer port on the rear panel go to the CPU Motherboard. A comments keyboard can be attached to another port on the Edit Controller for diagnostics or other applications.

2-3 Control Signal and Status Signal Flow

As shown in Figure 2-1, the PC AT I/O bus provides a data pipeline between the CPU and other PWAs in the bus slots. The bus signals are listed in Table 6-2. (Section six discusses the CPU Motherboard PWA.) The 8-Channel ILC PWA has a separate 80C186 CPU with a shared memory address space, and converts data to and from SMPTE serial format for communication with outside devices.

The main CPU processor communicates with the ACE 25 keyboard through an ILC channel, using the SMPTE Serial (ES Bus) protocol. Keystrokes and transport control knob position data are decoded and sent to the main CPU.

The Data Video Display PWA receives data from the CPU through the I/O bus, and converts it into video displays for the monitor. The ASCII characters are translated into dot patterns, then sent as video along with horizontal and vertical sync pulses to the video display monitor.

The CPU monitors video timing signals through the Color Frame 1 ID PWA, and uses this information to determine timing for switching video signals.

The ACE 25 system responds to operator input according to the program stored in RAM. For example, when a tape transport is selected for fast-forward operation, the keyboard command is decoded through the 8-Channel ILC PWA and passed to the main CPU, where the appropriate commands are determined, passed back to the 8-Channel ILC PWA, and sent to the tape transport. Status data from the transport is returned via the ILC PWA to the main CPU, which in turns sends data to the Data Video Display PWA to update the monitor display.

2-4 Audio/Video Signal Flow

Audio and video signals originate from a number of sources:

- Tape machines controlled by ACE 25
- Other sources (which can be controlled through GPI ports) such as ADO, ESS-5, or other video special effects systems
- Station reference black video

ACE 25 can be configured to control either composite or component video sources, and up to six audio sources with two channels each.

ACE 25 controls either external or internal audio and video switchers to select one audio source and one video source for the record VTR. If internal switchers are used, they are controlled directly by the CPU, and the audio and video signals are processed internally. If external switchers are used, then the audio and video signals are routed from the source machine through the switcher to the recorder. A separate effects generator such as an ADO 3000 may be added to the signal processing path.

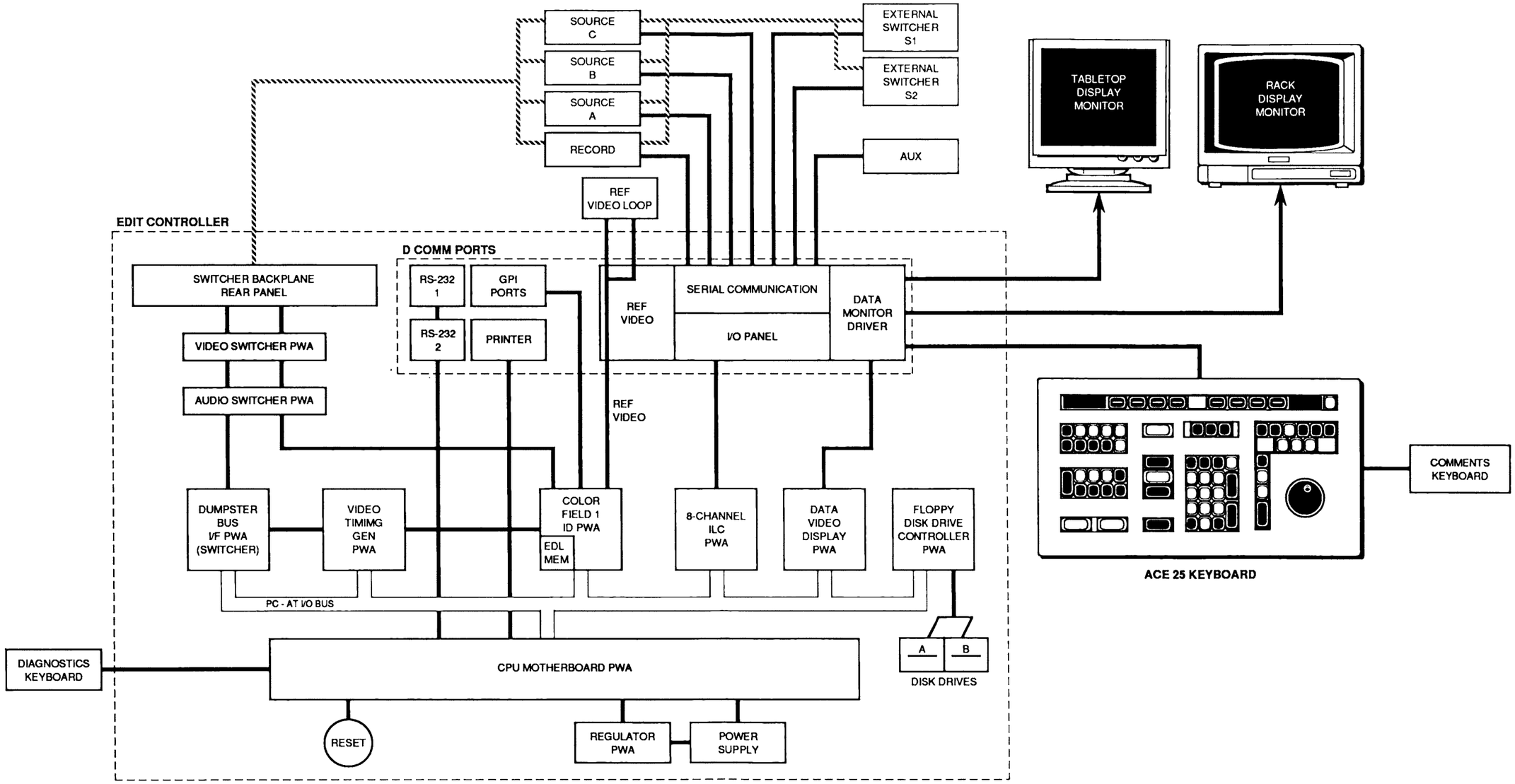


Figure 2-1.
System Block Diagram

2-5 SOFTWARE

All ACE 25 software is contained on the ACE 25 system disk, which is inserted into Drive 0 after the unit is turned on. This system disk contains the following programs: the primary ACE 25 program called QUATRO; the MS-DOS operating system; disk formatting programs, system configuration information, the ILC software (also known as the Worm program), VTR interface information, and miscellaneous programs.

2-6 Initialization

When the system is powered on (or manually reset), several initialization processes take place. The MS/DOS operating system is loaded from the system disk; MS/DOS then, in turn, loads the ACE 25 software. The 8-Channel ILC PWA is initialized and device drivers are loaded. Start-up diagnostic programs are run by the main CPU and by the ILC PWA CPU to check memory. When the process is complete, the display monitor presents a basic menu and the system is ready for operator action.

Figure 2-2 illustrates the initialization process. When ACE 25 is powered on, the system becomes an AT-type computer, and accesses the disk to enable the boot tracks to load the MS-DOS program. The MS-DOS program configures the system for devices (disk drives, memory size, etc.). The command processor is loaded next, and starts executing the AUTOEXEC. BAT file. AUTOEXEC is a small batch program that mimics keyboard input.

The AUTOEXEC file contains the initialization process. It loads and executes the ILC program , which transfers the Worm program to the ILC PWA to activate that board. The Worm program is a special software program that transfers itself with data from one host CPU to another host CPU. RAM diagnostics are run at power on or when the Worm program begins loading. A drive is created in RAM memory and a number of programs are loaded into it. Lastly, QUATRO, the main ACE 25 program, is loaded and starts execution.

The ILC PWA starts running ROM-based diagnostics at power-on. The Worm program triggers a hardware reset of the ILC PWA, and the diagnostics run again while the Worm waits. When completed, the Worm program transfers itself into the ILC memory, and begins execution. It sets up the ILC PWA for operation and establishes communication with the main CPU.

The QUATRO program performs some diagnostics, and checks the ILC PWA to see if it is operating correctly. QUATRO also initializes the pSOS operating system, which takes control and relegates MS-DOS to handling only disk access functions.

When the entire initialization procedure is complete, the screen displays the starting operator menu.

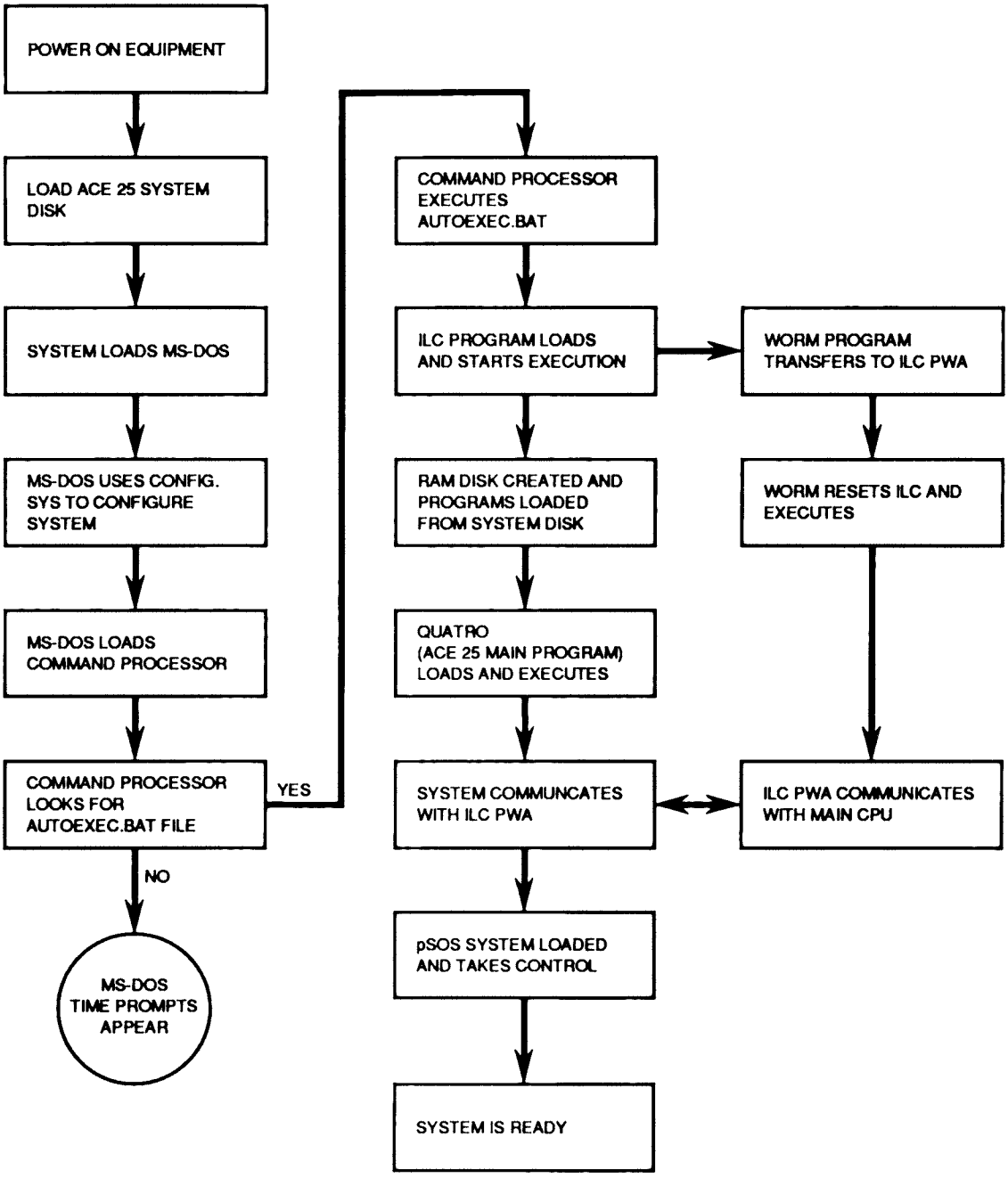


Figure 2-2. Initialization Process

2-7 Software Overall Block Diagram

Figure 2-3 is an overall block diagram of ACE 25 software. The main program (QUATRO), which is the central focus, interfaces with the Display Monitor, Timing Board, ILC Board, MS-DOS Disk Interface, and Keyboard software modules.

2-8 pSOS Operating System

The pSOS operating system is contained in the larger QUATRO program, and takes control at the end of initialization. The pSOS system has a number of sub-programs called processes, which interact with each other, and with other parts of the software/hardware system.

Figure 2-4 is a top-level data flow diagram of the system software. The diagram shows the flow of data through the system, the transformations performed on the data, and the processes which transform the data. The processes involved are "Interpret H/I Command," "Cook Keycodes," "Service DOS I/O," "Log Errors," and "Manage Human I/F Display." "ISR Run Real Time Tasks" is an interrupt service routine (ISR), not a process.

- "Interpret H/I Command" contains the system control software, and is the central, most active process; it accepts user command codes ("Cooked Keycodes") as input, does work requested, and farms out tasks to other processes as required.

  "Cook Keycodes" receives and processes raw keycodes to produce command packets, which are sent to the editing engine in "Interpret H/I Command" process. All soft keys and keyboard dependencies are removed. Commands are checked for immediate action, and acted on, when appropriate.
- "Service DOS I/O" performs all interfacing with MS/DOS I/O tasks, such as file I/O, disk utilities, and printer spooling.
- "Log Errors" performs tasks required to display and log all error messages. It contains formatting functions to customize error messages using parameters sent with error numbers, and keeps an error log containing time-stamped errors. Log in ASCII form can be requested by "Interpret H/I Command."
- "Manage Human I/F Display" performs display output tasks, and is separate from "Interpret H/I Command." Transport position and status information is updated regularly from "Audio/Video Src Database." "Manage Human I/F Display" implements window-based display system; however, users cannot change size or position of windows. Services of this process include:
  - Window Management (open, close, hide, expose)
  - Display strings at specified locations in windows
  - Update the contents of windows

  "Run Real-Time Tasks" performs operator input, and performs all RS-422 communications tasks, including receiving keyboard inputs and checking incoming error messages. Status messages from audio/video devices are used to keep "Audio/Video Src Database" current, while keyboard messages are sent to "Cook Keyboard."

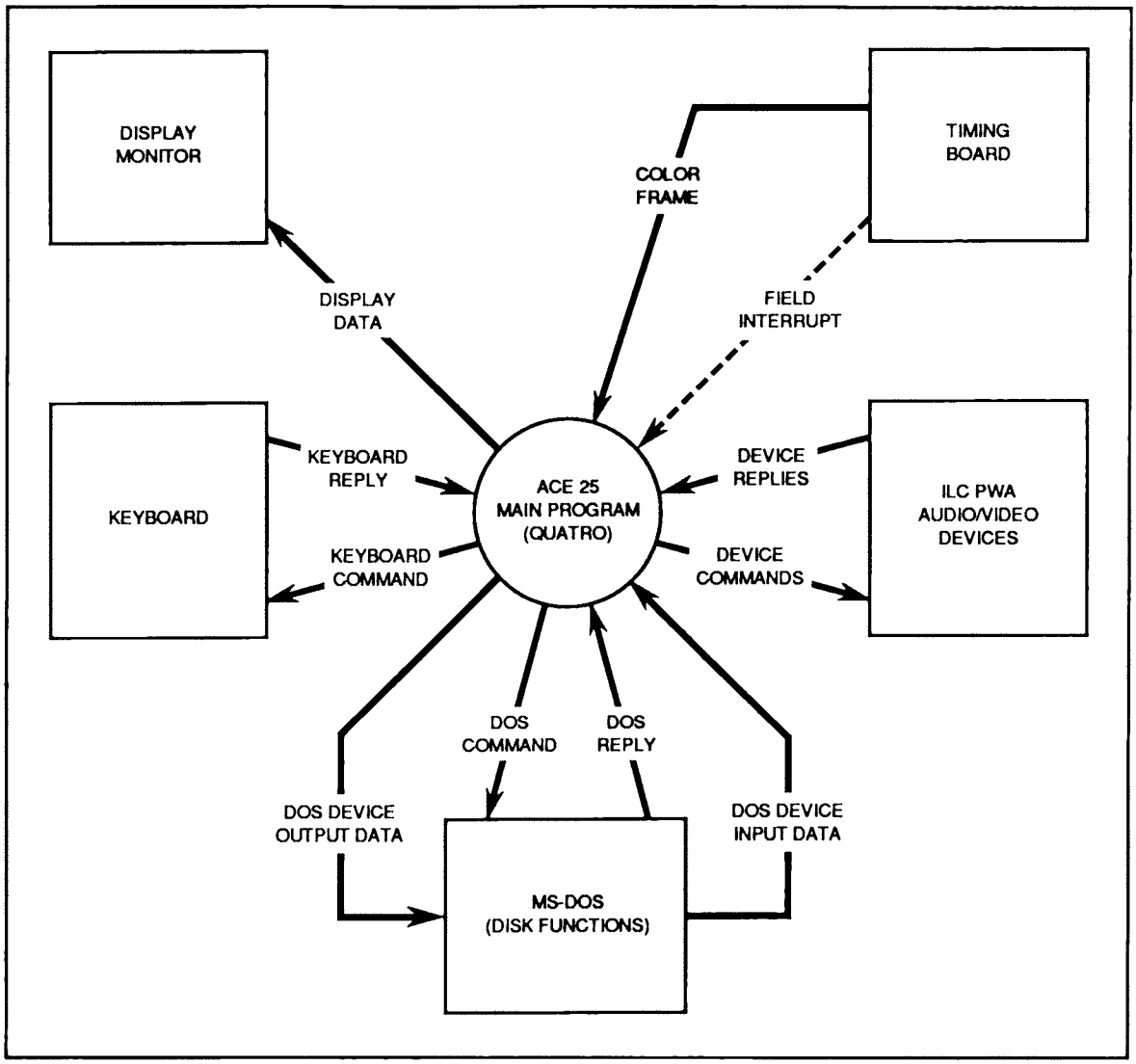


Figure 2-3. Software Overall Block Diagram

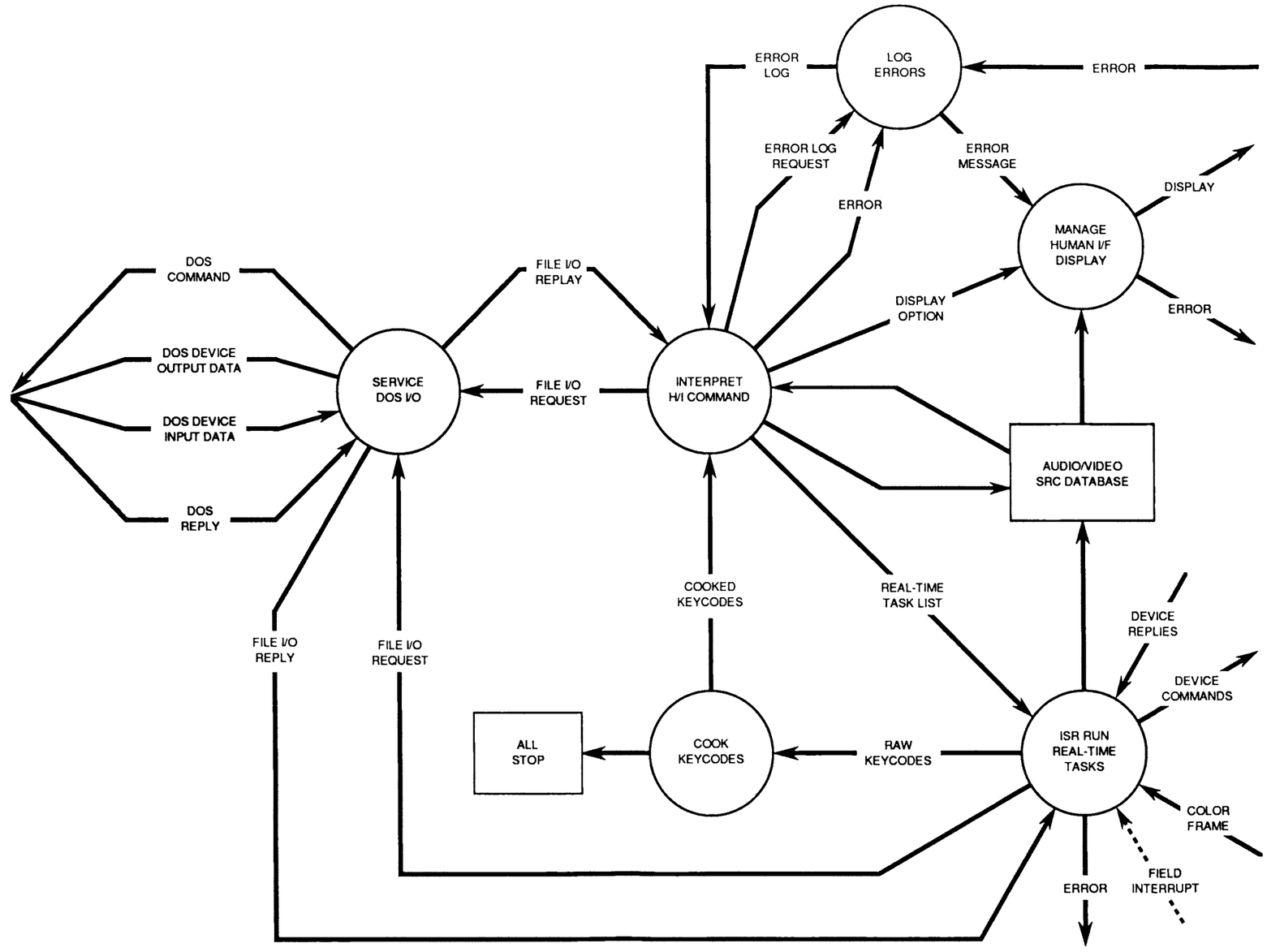


Figure 2-4.
Software Top Level Data Flow Diagram

SECTION 3

SYSTEM MAINTENANCE AND DIAGNOSTICS

3-1 INTRODUCTION

This section contains a list of recommended maintenance equipment, a performance check, routine preventive maintenance, system initial self-diagnosis messages, and set-up program information.

3-2 RECOMMENDED MAINTENANCE EQUIPMENT

Table 3-1 lists test equipment recommended for use in preventive and corrective maintenance procedures. If the recommended equipment is not available, substitute equipment with equivalent characteristics.

Table 3-1. Recommended Test Equipment

Equipment	Description
Audio Signal Generator	Tektronix ST1710
Cable, Coax (25)	BNC Connectors, 75Ω
Cable, Coax (10)	XLR Female to Mini XLLR Male
Cable, Coax (6)	XLR Male to Mini XLR Female
Color Monitor	Tektronix 655HR
Frequency Counter	Hewlett-Packard 5381A
Oscilloscope	Tektronix 465A
Probe, Oscilloscope (2)	Tektronix 6106
Vectorscope	Tektronix 520R
Video Distribution System	Dynair 5300
Video Signal Generator	Tektronix 140
Video Signal Generator	Tektronix 147
Video Signal Generator	Tektronix TSG300
Waveform Monitor	Tektronix 1485R
Waveform Monitor	Tektronix WFM300

3-3 PERFORMANCE CHECK

The following short procedure exercises key portions of the system and verifies , in part, that the system is operational. Checking every system function is time-consuming and does not significantly increase the probability of discovering improper operation.

Note

This procedure assumes that the operator or service person is familiar with system operation, as outlined in the *ACE 25 Operation* manual.

1. Load source recorders with pre-recorded tapes.
2. Load master recorder with blank tape or tape that contains expendable program material.
3. Turn on power to all units.
4. Insert the system program disk in Drive A and close the door. The disk drive should begin clicking and the disk drive front panel indicator should light. The initial screen display will be followed by the main system menu. If the prompt for setup appears, refer to paragraph 3-6.
5. Select source recorder A, then push PLAY on the ACE 25 keyboard. Check that source recorder A begins to operate in the play mode.
6. Select stop mode. Source Recorder A should stop.
7. Repeat steps 5 and 6 for other source machines.
8. Select source machine A, and mark entry and exit points on tape.
9. Stop source machine A, and select cut mode. The tape machine should rewind and roll to the cue point.
10. Select source machine B and mark entry and exit points. Select cut mode and cue machine to entry point.
11. Select preview mode. The source machines should role in sequence, causing video or audio from each source to be seen or heard on monitors.
12. If a switcher/effects generator is included in the system, repeat steps 9 through 11, using a dissolve of approximately 60 frames.
13. Repeat the edit, using a wipe pattern in place of the dissolve.
14. Roll the master machine and select an entry point.
15. Cue master machine to entry point.
16. Select edit mode. Source and master machines should roll, with source machine starting at the pre-selected points.

17. Select replay mode. The completed edit should appear on the monitors.

This completes the performance check.

3-4 ROUTINE PREVENTIVE MAINTENANCE

Inspect system at regular intervals (every 90 days is recommended at a minimum). Mechanical inspection and cleaning operations should be performed as follows:

1. Clean all exterior surfaces of units with a lint-free wipe moistened with 91 isopropyl alcohol.

2. Power-off all equipment, inspect interior of Edit Controller and CRT (remove covers), then use dry, low-pressure (20 psig) compressed air to remove dust accumulation. If necessary, use a soft-bristled brush to help remove dust.

3. Inspect air filter in front door of Edit Controller for dust accumulation. Replace or wash filter in warm, soapy water. Rinse thoroughly and replace when dry.

4. Inspect all connections and tighten if necessary. Inspect cables for abrasion or damage and replace as needed.

3-5 SYSTEM INITIAL SELF-DIAGNOSIS

ACE 25 software performs a self-diagnosis routine during initialization. If a problem is detected, the system produces a warning signal or fault message. Table 3-2 lists these warning signals and fault messages. If the system software detects that ACE 25 is not operating correctly, an operator error message is generated to alert the operator to the problem. Operator error messages are described and listed in Appendix A.

Table 3-2. Initial Self-Diagnosis Warning Signals and Fault Messages

Warning Signal	Suggested Action
Nothing happens	Check power supply and ac power cord
Continuous beep	Check power supply
Repeating short beeps	Check power supply
1 long beep, 1 short beep	Check CPU Motherboard PWA
1 long beep, 2 short beeps	Check Display Monitor
No display	Check Display Monitor
Fault Message	
101, 131	Check CPU Motherboard PWA
201	Check RAM on CPU Motherboard PWA
xxxx201 and Parity Check x	Check RAM on CPU Motherboard PWA
Parity Check x	Check Power Supply
301, xx031	Check ACE 25 keyboard
601	Check floppy disk drives
1701	Check Hard Disk Drive (not implemented)
1801	Check I/O Bus Slots on CPU Motherboard PWA

3-6 RUNNING THE SET-UP PROGRAM

The set-up display for initial machine setup appears when the ACE 25 is powered on and any of the following conditions occur:

- Battery low
- Date/Time Information missing or lost
- System Configuration missing or lost

ACE 25 stores basic start-up information in CMOS memory with battery backup. If this data is lost, ACE 25 will not operate. To restore this data, the SETUP UTILITY program must be run.

To run the SET UTILITY program:

1. Turn off the ACE 25.
2. Connect an IBM AT-compatible keyboard to the DIN connector on the rear panel of the ACE 25 Edit Controller unit.
3. Turn on the ACE 25.
4. Perform the following interactive sequence, where DISPLAY indicates the message displayed by ACE 25, and ENTER indicates the operator input:

DISPLAY:	Want to run Setup utility (Y/N)?_
ENTER:	Y
DISPLAY:	Current Date is: 11-25-1988 Enter new date (MM-DD-YY)? _
ENTER:	(Current date in MM-DD-YY format, where MM is the number of the month, DD is the number of the day of the month, and YY is the last two digits of the year)
DISPLAY:	Current Time is: 13:42:14 Enter new time: (HH:MM:SS)?_
ENTER:	(Current time in HH:MM:SS format, where HH is the number of hours based on a 24-hour system, MM is the number of minutes, and SS is the number of seconds.)

DISPLAY: Primary Display is: Monochrome display.

Fixed disk drive C type	: Not installed
Fixed disk drive D type	: Not installed
Diskette drive A is	: 3-1/2-inch drive
Diskette drive B is	: 3-1/2 inch drive
Base memory size is	: 640 KB
Expansion memory size	: 384 KB

Are these options correct (Y//N)?_

If options are correct,

ENTER: Y
[RETURN]

If options are not correct,

ENTER: N
[RETURN]
(Correct set-up parameters.)

SECTION 4

REPLACEMENT OF EDIT CONTROLLER ASSEMBLIES

4-1 INTRODUCTION

This section presents the procedures for removing and replacing major assemblies in the Edit Controller unit. For some machines, parts may be different from those described; consult field service bulletins and change notices for more information.

WARNING

POWER OFF EDIT CONTROLLER UNIT BEFORE REMOVING COMPONENTS.

4-2 TOP COVER REMOVAL

The top cover is secured by 18 cross-recessed screws, shown in Figure 4-1. The following procedure is used to remove the top cover:

1. Lower front cover and loosen 4 cross-recessed screws in front (see Figure 4-1 [A]).
2. Remove 4 cross-recessed screws on rear lip of top cover (see Figure 4-1 [B]).
3. Loosen 10 cross-recessed screws (5 on each side of cover). (See Figure 4-1 [C].)
4. Lift top cover from Edit Controller chassis.

To replace cover, reverse the above procedure.

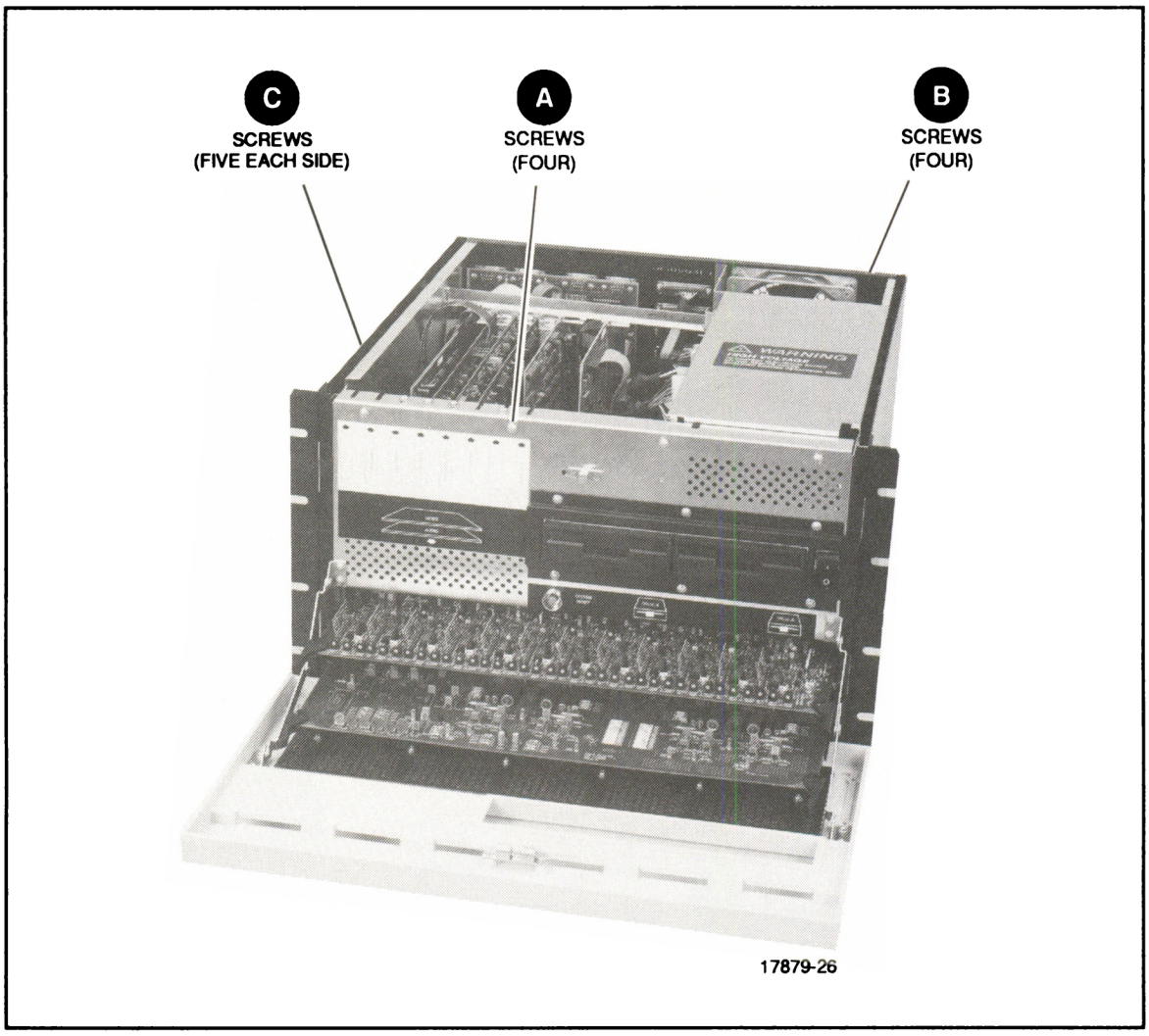


Figure 4-1. Edit Controller - Top Cover Removal

4-3 POWER SUPPLY REMOVAL

Note

Check Power Supply fuse before removing Power Supply.

The following procedure is used to remove the Power Supply. See Figure 4-2.

1. Turn off power and unplug power cord from Edit Controller unit.
2. Remove Top Cover (refer to Paragraph 4-2).
3. Remove two cross-recessed screws (opposite fan at rear end of power supply).

   Slide Power Supply shield plate off.
4. Carefully separate plastic connector. Refer to Figure 4-2 [A].
5. Label 110 Vac and 220 Vac leads, then remove leads from jacks on power supply.

   (See Figure 4-2 [B].)
6. Label 3 leads on terminal strip (see Figure 4-2 [C]), then loosen screws and remove leads.
7. Loosen 8 screws securing leads at terminal strip (see Figure 4-2 [D]), then remove leads.
8. Remove 5 screws securing Power Supply (see Figure 4-2 [E]).
9. Carefully lift Power Supply out of Edit Controller unit.

To replace Power Supply, reverse the above procedure.

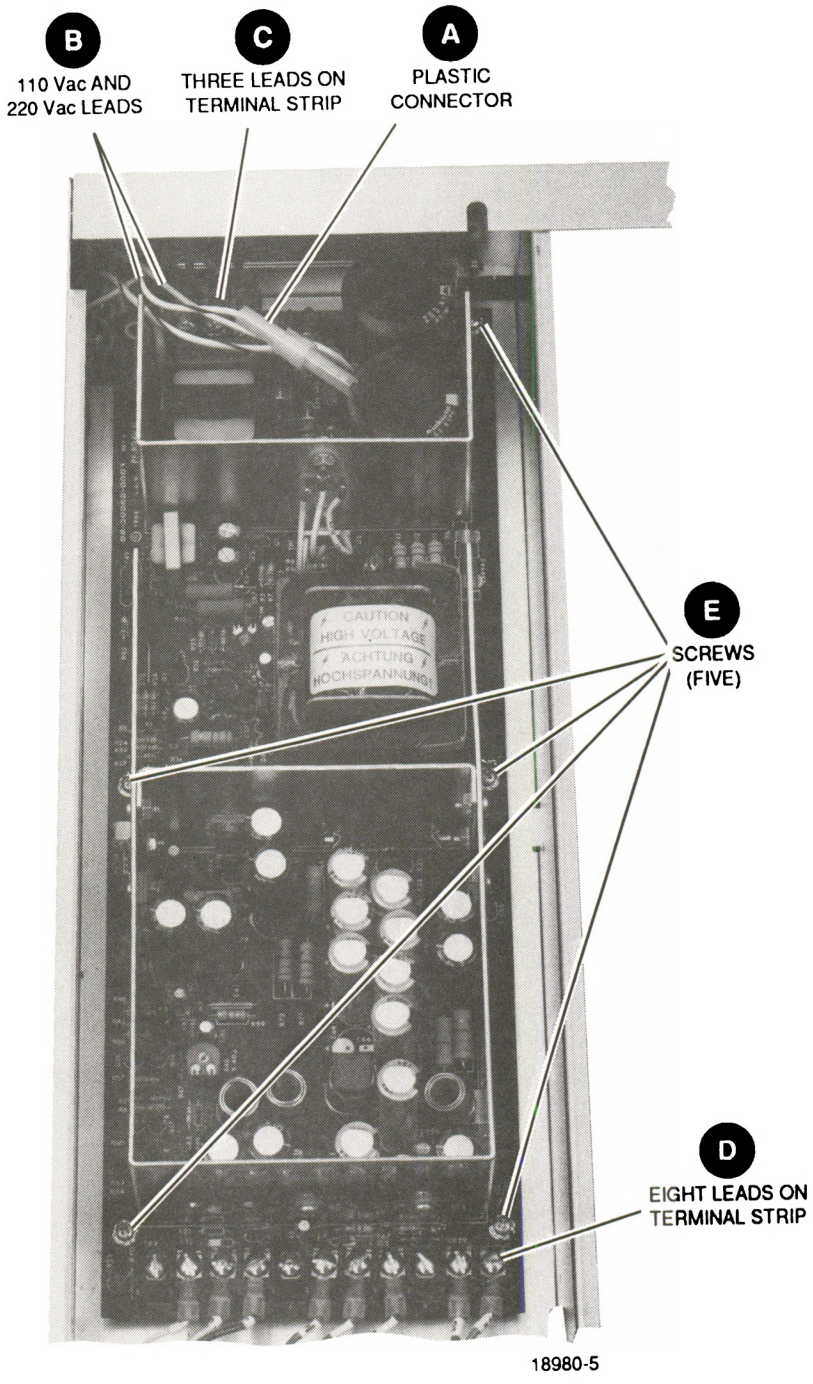


Figure 4-2. Edit Controller Power Supply Removal

4-4 DISK DRIVE ASSEMBLY REMOVAL

The following procedure is used to remove the Disk Drive Assembly:

1. Remove disks from disk drives.
2. Turn off power to Edit Controller unit.
3. Remove Top Cover (refer to paragraph 4-2).
4. Remove flat cable connected to Disk Controller PWA from board. Leave other end connected to Disk Drive Assembly.
5. Remove connector J5 on Regulator PWA (power leads to Disk Drive Assembly).
6. Remove cross-recessed screw on tab at rear of drives next to Regulator PWA.
7. Remove 6 cross-recessed screws from front panel securing Disk Drive Assembly.
8. Carefully pull Disk Drive Assembly out of Edit Controller unit from front.

To replace Disk Drive Assembly, reverse above procedure.

The following procedure is used to remove individual drives from the assembly. See Figure 4-3.

1. Unplug power cable from rear of drive.
2. Unplug flat cable from rear of drive.
3. Turn Disk Drive Assembly upside down.
4. Remove 4 cross-recessed screws securing drive to be removed.
5. Remove drive through front slot in Disk Drive Assembly frame.

Note

When replacing drives, make sure drive designation switch is correctly set. Refer to Section 7 for details.

Reverse above procedures to replace Disk Drive Assembly in Edit Controller chassis.

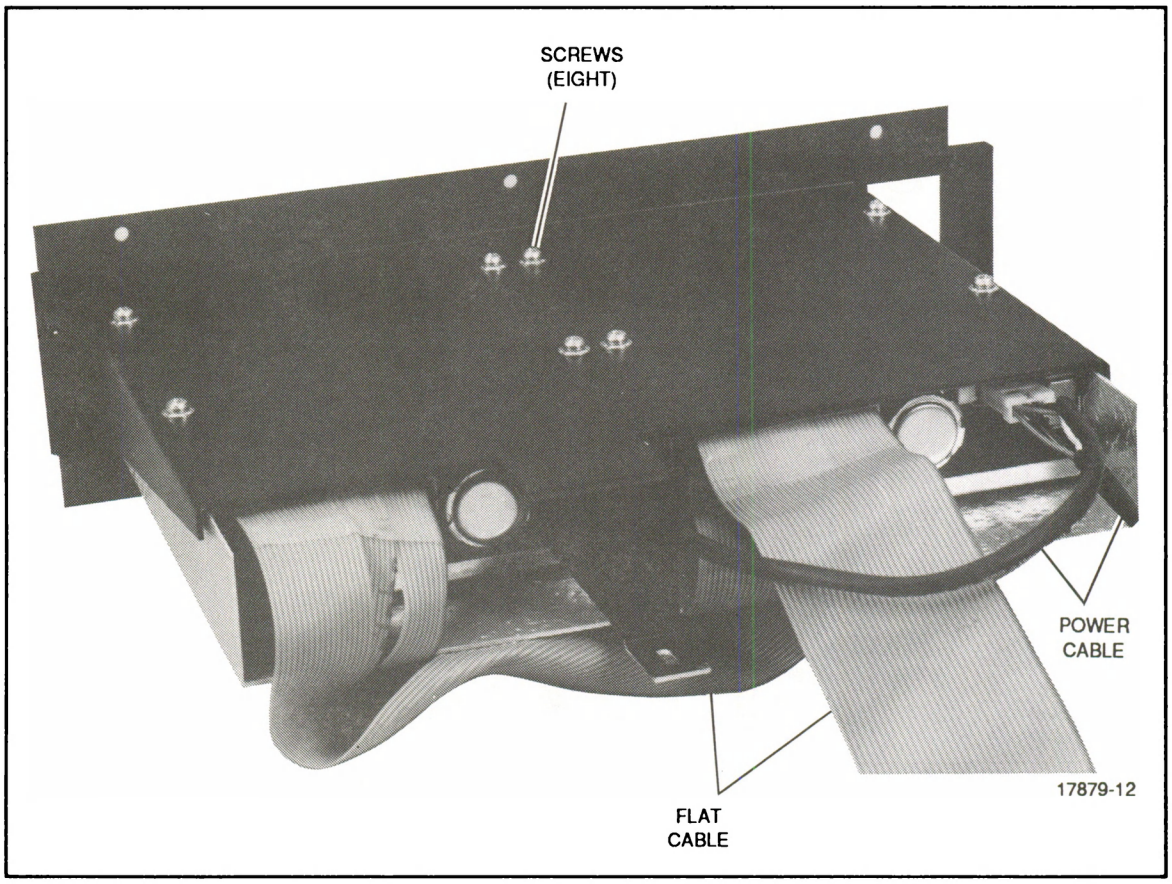


Figure 4-3. Disk Drive Assembly

4-5 PWA REMOVAL

The following procedure is used to remove PWAs from the I/O bus slots of the CPU Motherboard PWA. See Figure 4-4.

1. Turn power off for Edit Controller unit and remove power cord.
2. Remove Top Cover (refer to paragraph 4-2).
3. Remove 2 cross-recessed screws securing bar holding PWAs in place. See Figure 4-4 [A].

Note

These 2 screws may be difficult to remove.

4. Remove bar by lifting end attached to shielding for Power Supply (see figure 4-4 [B]).
5. Remove any cables attached to PWA to be removed.
6. Carefully remove PWA by pulling up on metal tab attached to PWA (see Figure 4-4 [C]).

To replace PWA, reverse above procedure.

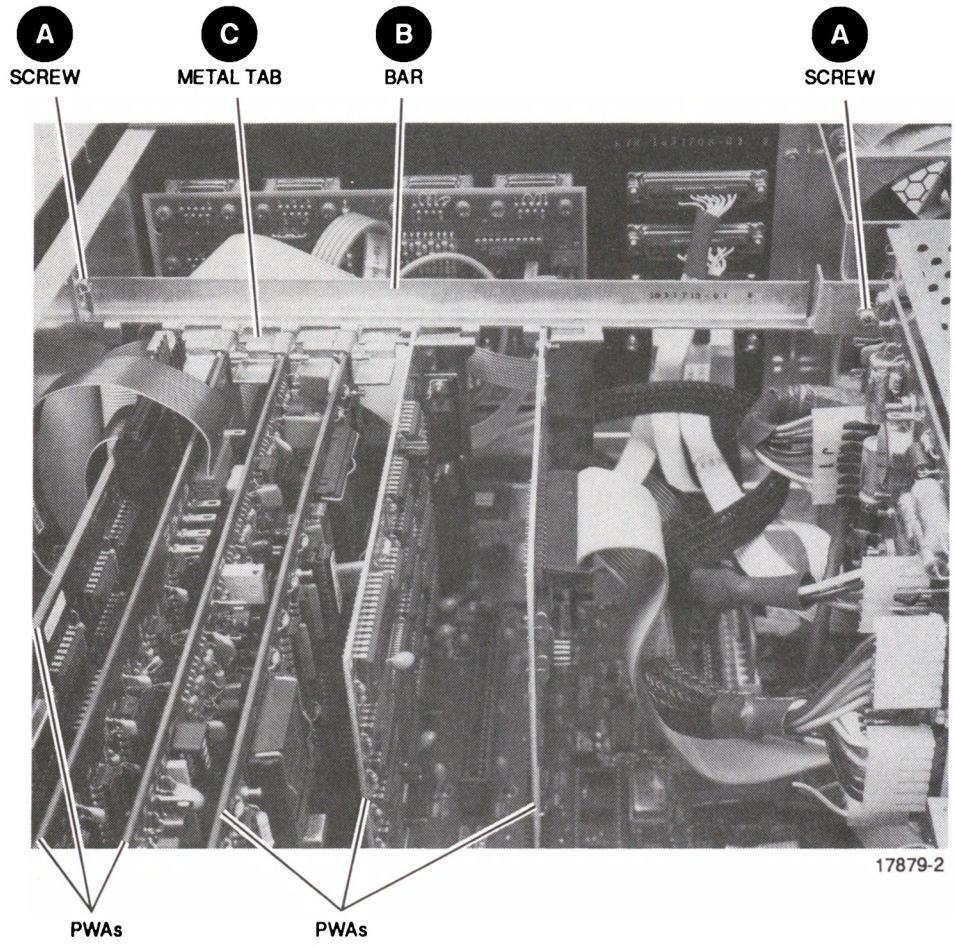


Figure 4-4. PWA Removal

4-6 REGULATOR PWA REMOVAL

The following procedure is used to remove the Regulator PWA. See Figure 4-5.

1. Turn off power and unplug power cord from Edit Controller unit.
2. Remove Top Cover (refer to paragraph 4-2).
3. Remove one or more PWAs as necessary (see Paragraph 4-5) to permit easy access to Regulator PWA.
4. Unplug connector J1 on Regulator PWA for cable from Power Supply (see Figure 4-5 [A]).
5. Unplug connector J3 on Regulator PWA for leads from dc Fan (see Figure 4-5 [B]).
6. Unplug connector J4 on Regulator PWA from Switcher Backplane Assembly (see Figure 4-5 [C].
7. Unplug connector J5 on Regulator PWA from ON/OFF switch (see Figure 4-5 [D]).
8. Unplug connectors J8 and J9 on Regulator PWA from CPU Motherboard PWA (see Figure 4-5 [E]).
9. Remove 4 cross-recessed screws securing Regulator PWA to side of Power Supply shielding (see Figure 4-5 [F]).
10. Carefully remove Regulator PWA.

To replace Regulator PWA, reverse above procedure.

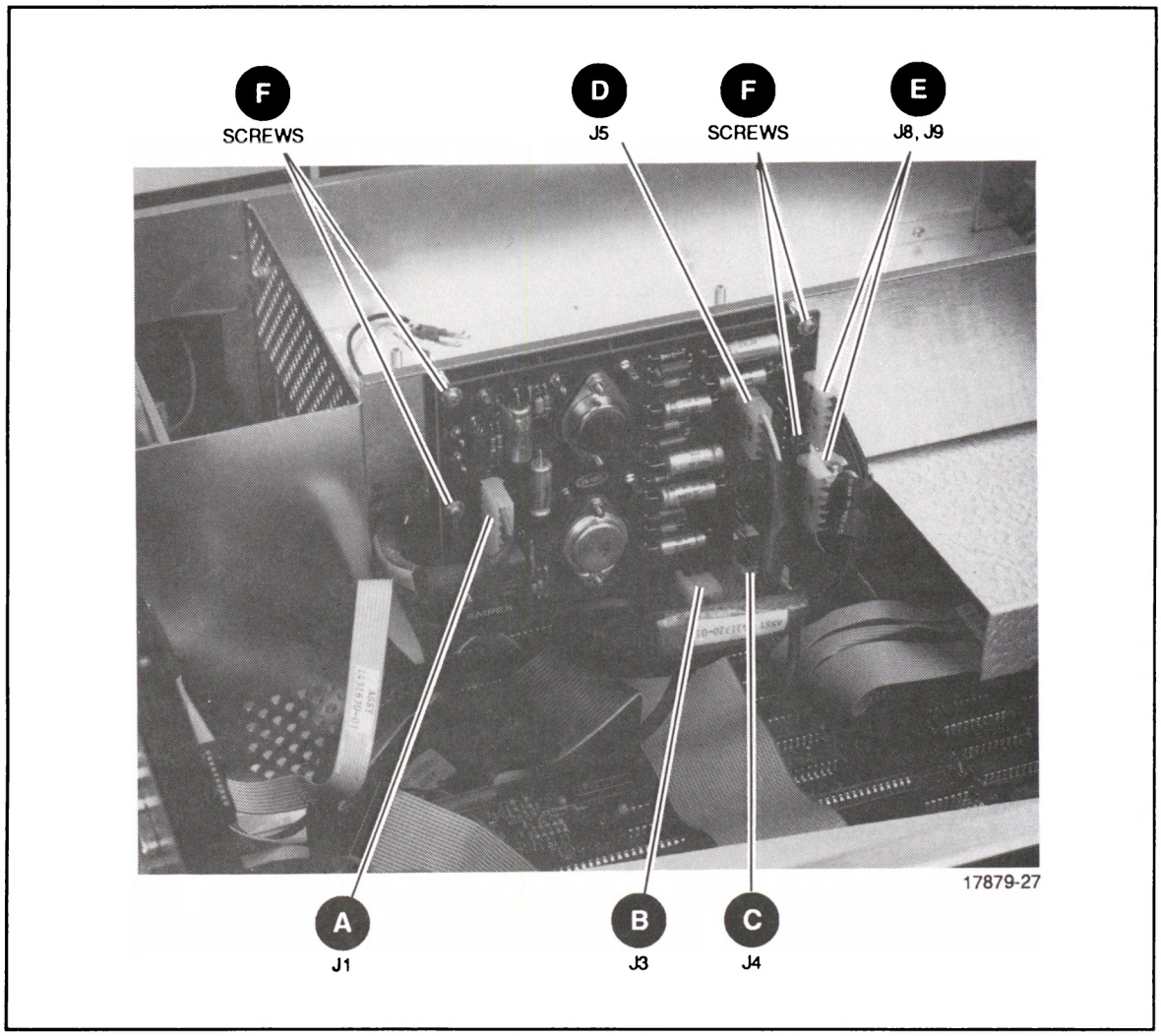


Figure 4-5. Regulator PWA Removal

4-7 INPUT/OUTPUT PANEL REMOVAL

The following procedure is used to remove the entire Input/Output Panel Assembly, which includes the Input/Output PWA, Fuseholder/ac receptacle, and dc Fan Assembly.

1. Turn power off on Edit Controller unit.
2. Remove all cables from rear panel of Edit Controller.
3. Remove Top Cover (refer to paragraph 4-2).
4. Remove Power Supply Shield Cover (refer to paragraph 4-3).
5. Remove Disk Drive Assembly (refer to paragraph 4-4).
6. Remove 2 cross-recessed screws securing ON/OFF Switch on front panel.

7. Pull ON/OFF Switch out and label leads. Remove switch from 4 leads.

8. Separate plastic connector on Power Supply (see Figure 4-2 [A]).

9. Label 110 Vac and 220 Vac leads to Power Supply and remove 2 leads. (See Figure 4-2 [B].)

10. Label 3 leads to terminal strip. Loosen screws and remove leads. (See Figure 4-2 [C].)

11. Push leads removed in Steps 8, 9 and 10 down through gap under Power Supply shielding.

12. Remove ground lead from Fuseholder/ac Receptacle at rear of Power Supply shielding.

13. Remove connector J5 on Regulator PWA (leads from dc Fan). Pry rubber bushing around leads out of hole. Feed leads and connector through hole.

14. Remove connectors J9 and J7 (for Serial ports) on CPU Motherboard PWA. When replacing leads, make sure Serial Port 1/3 is on J9 and Serial Port 2/4 is on J7.

15. Remove connector J8 (flat black cable for printer) from CPU Motherboard PWA.

16. Remove connector J4 (round metal 5-pin connector for Diagnostic Keyboard) from CPU Motherboard PWA.

17. Remove cable and connector from Monochrome Video Display PWA.

18. Remove BNC connector from Color Field 1 Identifier PWA.

19. Remove cable and connector from Input/Output PWA for GPIs (from Color Field 1 Identifier PWA).

20. Remove 10 cross-recessed screws on outside of Input/Output Panel Assembly securing panel to chassis. (Make sure the two screws in the middle of panel are removed.)

21. Lift slightly to clear lip of Switcher Interface Panel, and carefully pull Input/Output Panel up and away, then lay flat to access remaining cables.

22. Remove connector J9 and cable on Input/Output PWA (flat cable to 8-Channel ILC PWA).

23. Pry rubber bushing around cable to ON/OFF Switch out of hole, and pull cable through hole.

24. Carefully remove entire Input/Output Panel Assembly from Edit Controller chassis. Figure 4-6 shows the Input/Output Panel Assembly after removal.

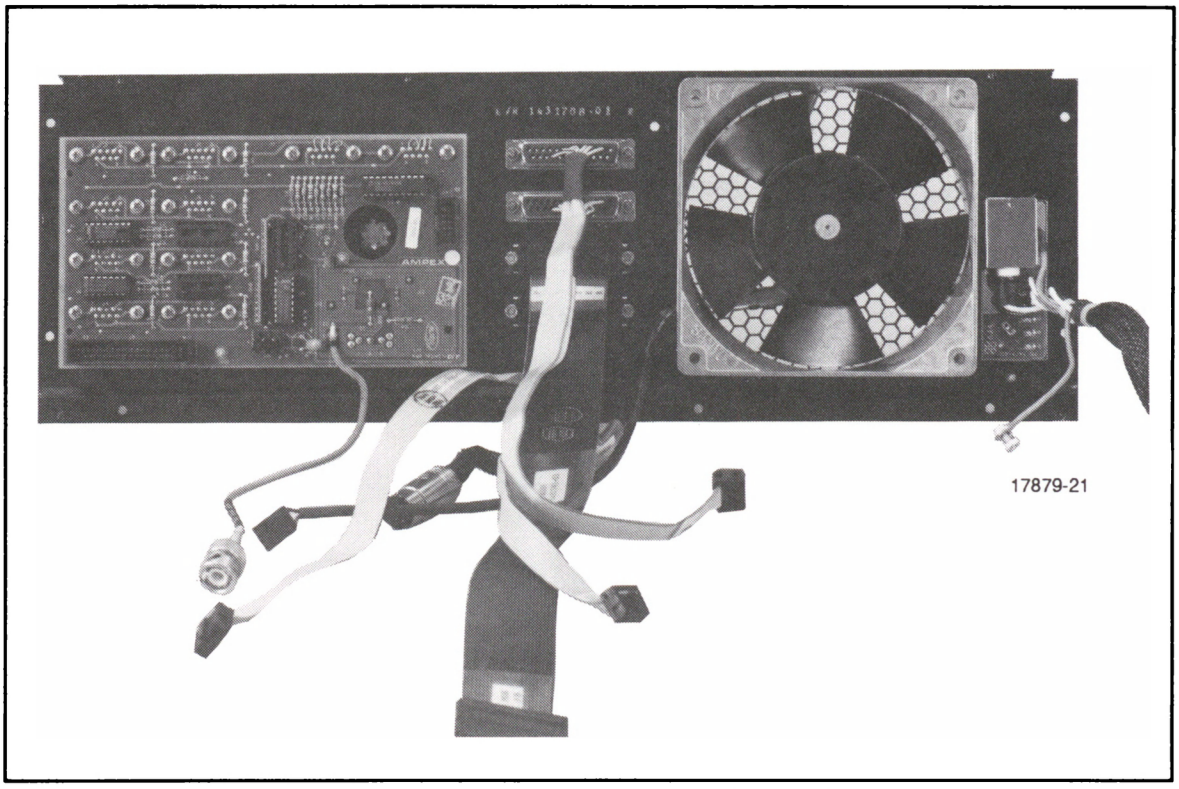


Figure 4-6. Input/Output Panel Assembly

To remove the Input/Output PWA from the panel:

1. Remove hex-head screws from 10 RS-422 connectors.
2. Remove nuts securing both BNC video connectors.
3. Carefully remove Input/Output PWA from assembly.

To replace Input/Output PWA and Input/Output Panel Assembly, reverse above procedures.

4-8 SWITCHER BACKPLANE ASSEMBLY REMOVAL

The following procedure is used to remove the Switcher Backplane Assembly:

1. Turn power off to Edit Controller unit.
2. Disconnect all cables on rear of Switcher Backplane Assembly.
3. Lower front cover and pull switcher boards (if installed) out approximately 2-3 inches.
4. Remove Top Cover from Edit Controller unit (refer to paragraph 4-2).
5. Remove 5-pin connector and cable on Switcher Backplane PWA (from Video Timing PWA).
6. Remove connector and large flat cable connected to Dumpster Bus Interface PWA.
7. Remove connector and small cable connected to Edit Controller chassis.
8. Remove cross-recessed screws securing Switcher Backplane Assembly to Edit Controller chassis.
9. Gently pull entire assembly from chassis, pulling attached cables through slot inside chassis.

Figure 4-7 shows the Switcher Backplane Assembly after removal.

To replace the Switcher Backplane Assembly, reverse above procedure.

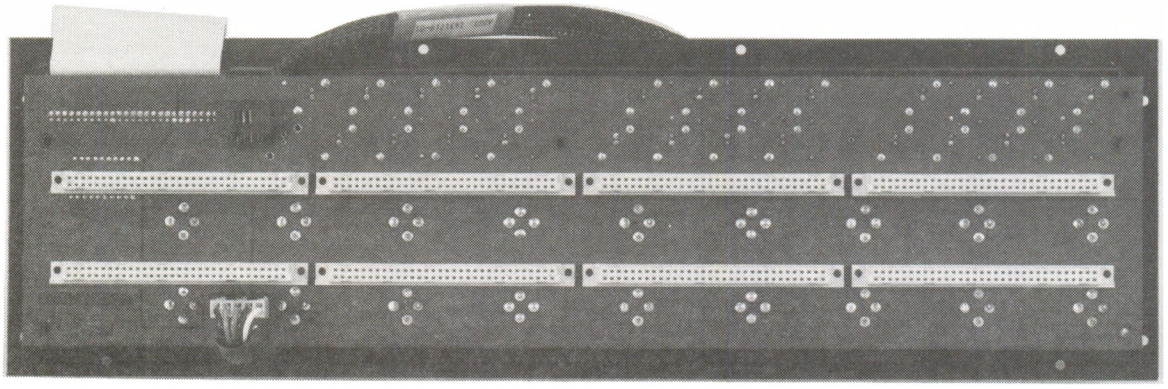


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Figure 4-7. Switcher Backplane Assembly

4-9 CPU MOTHERBOARD PWA REMOVAL

The following procedure is used to remove the CPU Motherboard PWA. Figure 4-8 shows this board in the Edit Controller chassis.

1. Turn off power for Edit Controller unit.
2. Remove top cover from Edit Controller unit (refer to paragraph 4-2).
3. Remove Disk Drive Assembly (refer to Paragraph 4-4).
4. Remove PWAs in slots in CPU Motherboard PWA (refer to paragraph 4-5).
5. Remove connector J12 to Reset Switch (see Figure 4-8 [A]).
6. Remove connector on CPU Motherboard PWA to External Battery (W15).
7. Remove Diagnostic Keyboard Connector (J4) on CPU Motherboard PWA.
8. Remove connectors J4 and J5 on the CPU Motherboard PWA (to Regulator PWA).
9. Remove connectors J7 and J9 on CPU Motherboard PWA (Serial Ports 1/3 and 2/4).
10. Remove connector J8 to Input/Output Panel.
11. Remove 6 cross-recessed screws securing PWA to Edit Controller (see Figure 4-8 [B]).
12. Tilt PWA and carefully remove from Edit Controller chassis. Watch out for metal tab (see Figure 4-8 [C]).

4-10 FRONT COVER ASSEMBLY REMOVAL

Figure 4-9 shows the Front Cover Assembly in lowered position prior to removal. The following procedure is used to remove the Front Cover:

1. Open Front Cover.
2. Remove 2 cross-recessed screws securing Front Cover support on each side.
3. Remove 7 cross-recessed screws securing Front Cover hinge to Edit Controller chassis.
4. Remove Front Cover Assembly.

To replace Front Cover Assembly, reverse above procedure.

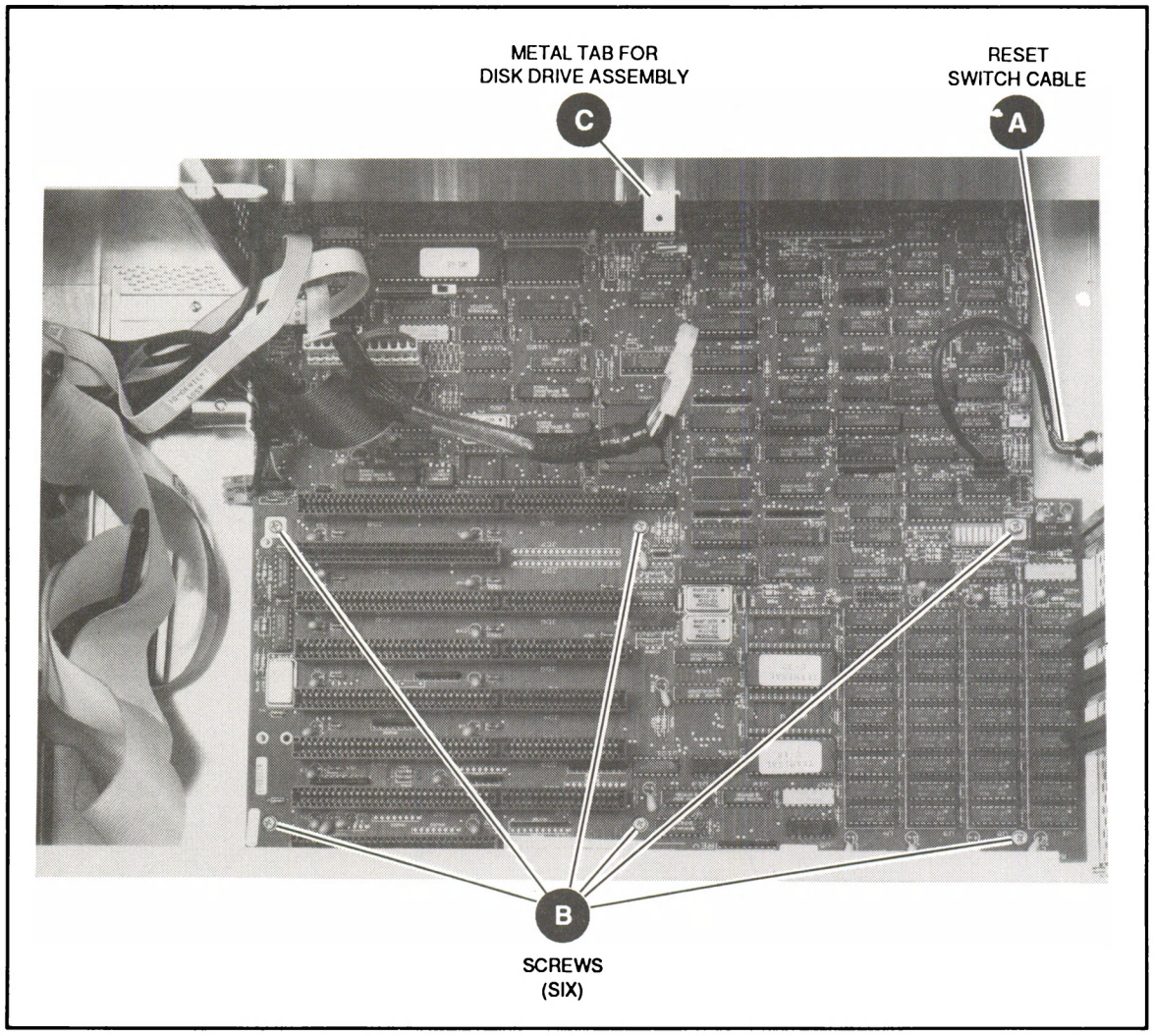


Figure 4-8. CPU Motherboard PWA in Edit Controller Chassis

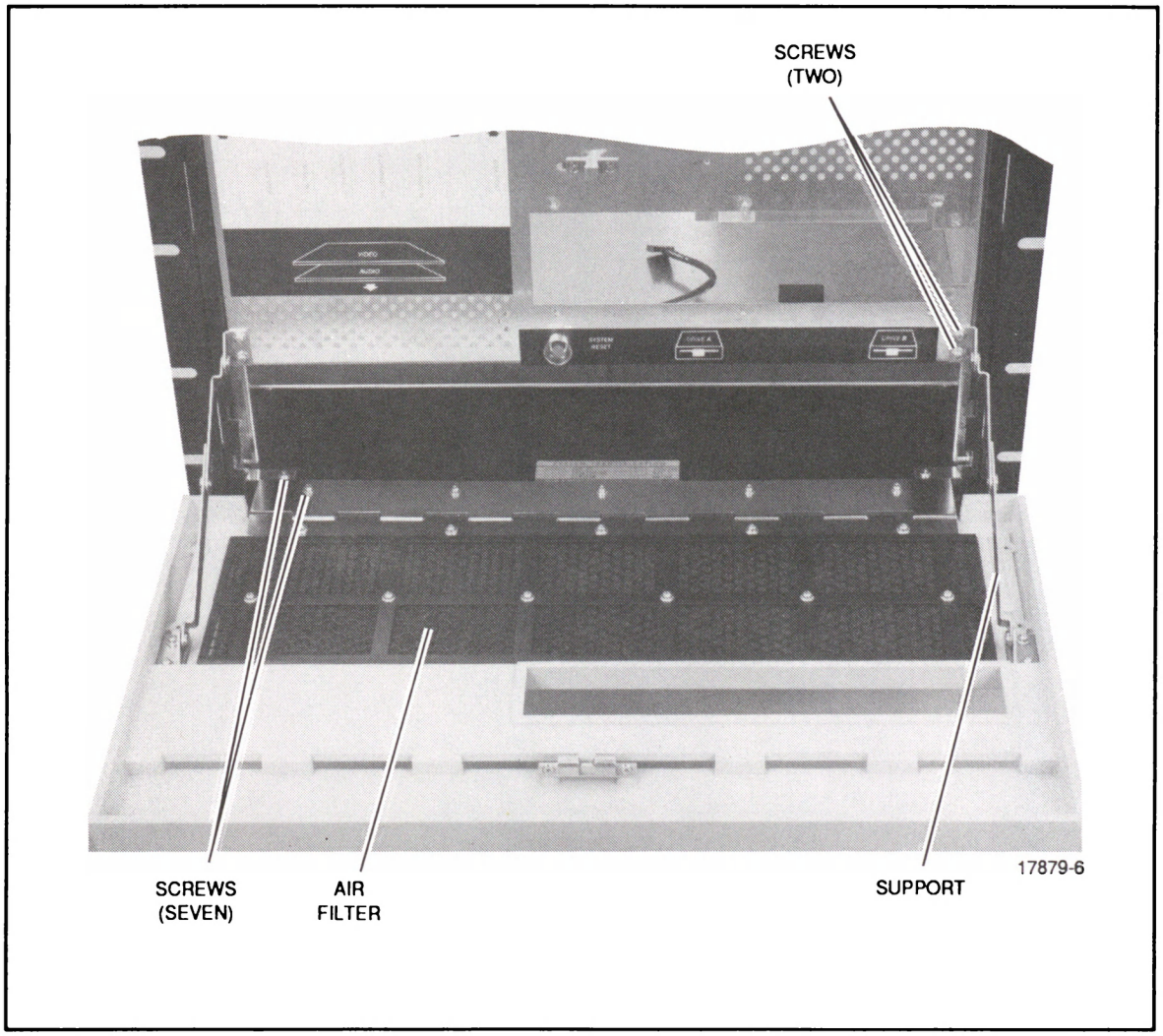


Figure 4-9. Front Cover Assembly

SECTION 5

POWER AND COOLING

5-1 INTRODUCTION

This section covers the power and cooling systems in the ACE 25. The following items are discussed in the order listed:

- Power requirements, power consumption, and temperature/humidity requirements
- Ac power receptacle/fuseholder and main ON/OFF switch
- Power supply and Regulator PWA, including appropriate test points and adjustments
- dc fan assembly

5-2 POWER REQUIREMENTS, POWER CONSUMPTION AND OPERATING CONDITIONS

Power requirements, power consumption, and recommended operating conditions are covered in the following paragraphs.

5-3 Power Requirements

The ACE 25 system can be configured to one of two different power standards:

- 90-132 Vac, 47-63 Hz single phase
- 180-264 Vac, 47-63 Hz single phase

The edit controller unit, keyboard, and data monitor have separate power connections (3-prong grounded). The rack-mounted monitor unit (optional) also requires a separate connection. Each unit of equipment is separately fused.

5-4 Power Consumption

The estimated power consumption for each unit of ACE 25 is:

Edit Controller: 1 amp at 110 Vac; 0.5 amp at 220 Vac

Keyboard: .25 amp at 110 Vac; .13 amp at 220 Vac

Data Monitor: .7 amp at 110 Vac; .35 amp at 220 Vac

Power consumption of the Edit Controller unit will be higher when internal switchers are installed.

5-5 Operating Conditions

The following temperature/humidity conditions are recommended:

Maximum operating temperature: 40° C ambient

Minimum operating temperature: 10° C ambient

Relative humidity (non-condensing): 10-90%

Normal operating temperature range: 15-27° C ambient

Normal humidity (non-condensing) : 80%

5-6 AC POWER RECEPTACLE/FUSEHOLDER, AC HARNESS AND MAIN ON/OFF SWITCH

The ac electrical system includes the AC Power Receptacle/Fuseholder, AC Harness and the Main ON/OFF Switch, which are discussed in the following paragraphs.

5-7 AC Power Receptacle/Fuseholder

The AC Power Receptacle/Fuseholder (P/N 145-708) is located on the upper rear panel of the Edit Controller unit (see Figure 5-1). The top part is the receptacle for the ac power cord (3-prong grounded). The lower part is the fuseholder, with the selected voltage read off the Line Voltage Select PWA. The fuse used is:

120 Vac: 3 amp

240 Vac: 1.5 amp

To change voltage:

1. Remove power cord and slide plastic cover over fuse connector up.
2. Pull small handle to partially raise fuse. Remove fuse.
3. Insert needle-nose pliers in hole in circuit board, and remove circuit board.
4. Position board so correct line voltage can be read (120V or 240V) when board is inserted .

WARNING

DO NOT USE 100 OR 220 POSITIONS.

5. Install correct fuse for voltage and close fuse cover. Replace power cord.

Note

The ground wire (green) is connected to the metal shielding screen at the rear of the power supply.

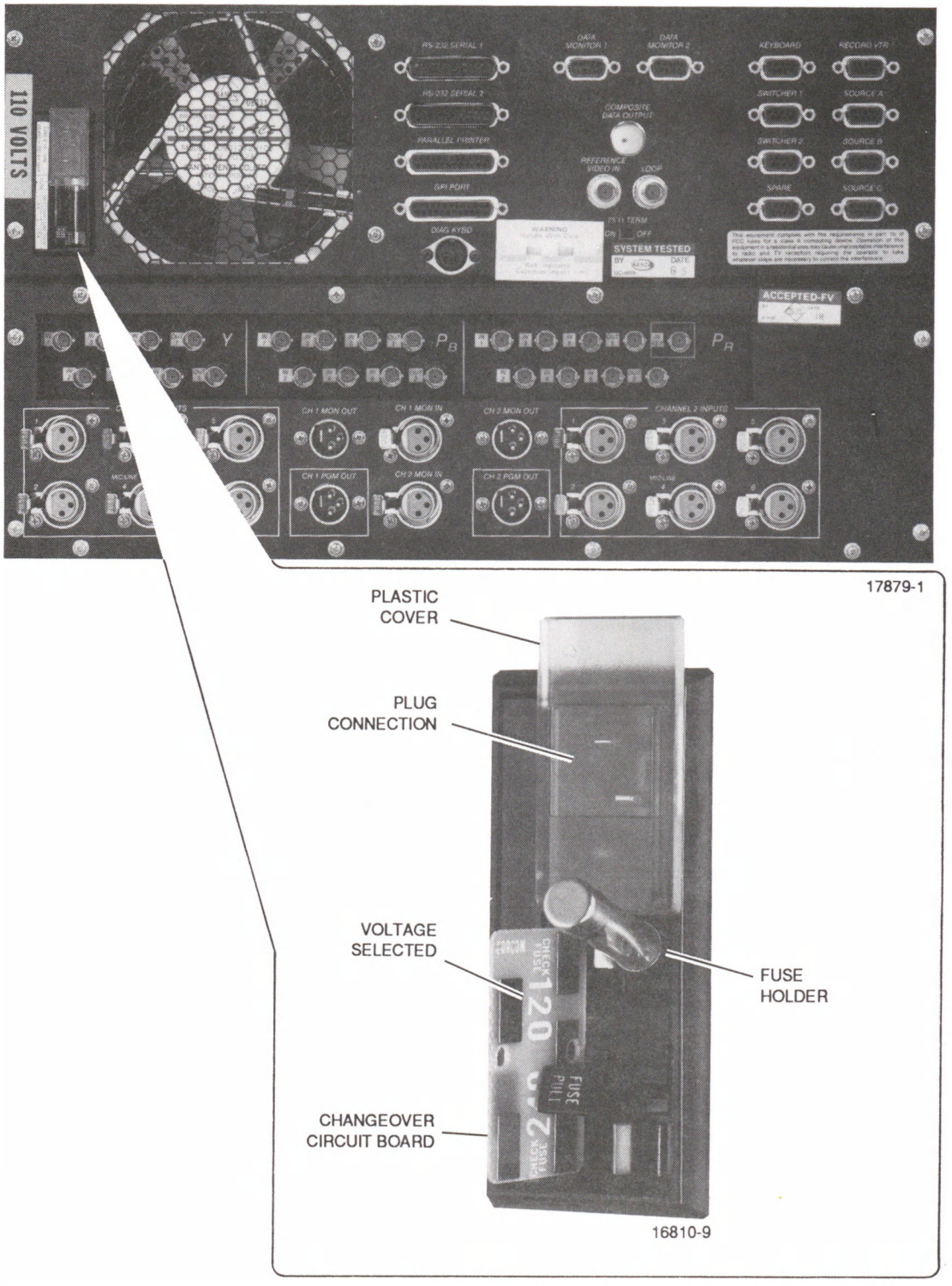


Figure 5-1. Edit Controller Fuse Holder

5-8 AC Harness

The primary AC wiring harness (P/N 1430879) with connections, is shown in Figure 5-2. This harness connects the AC Power Receptacle/Fuseholder to the main ON/OFF switch and the power supply. This harness is run in the cavity under the power supply.

5-9 Main ON/OFF Switch

The main ON/OFF switch is located behind the front panel door, on the right hand side of the Edit Controller unit (see Figure 5-3). This switch is used to turn the ACE 25 Edit Controller on or off; it does not control power to the display monitor.

5-10 POWER SUPPLY (CONDOR)

The Condor power supply (P/N 1431581) is found in certain ACE 25 systems; other systems contain an SSI-type power supply (see paragraph 5-11). Figure 5-4 identifies the location of fuses, the LED, terminal strips, connections, test points and adjustment points. Table 5-1 lists the terminal strip contacts. The red LED is lit during normal operation. Adjust the power supply as follows:

WARNING

DO NOT ADJUST R34.

1. Attach voltmeter probe to pin 10 of U87 on the CPU Motherboard PWA.
2. Adjust R48 on power supply (see Figure 5-4) to achieve a +5.1 V reading on the voltmeter. R48 controls the +5 V output from the power supply.
3. Disconnect voltmeter probe.

This power supply contains two fuses (see Figure 5-4) with the following ratings:

Fuse 1: 5.0 amp, 3AG

Fuse 2: 2.0 amp, 5 mm x 20 mm (small size)

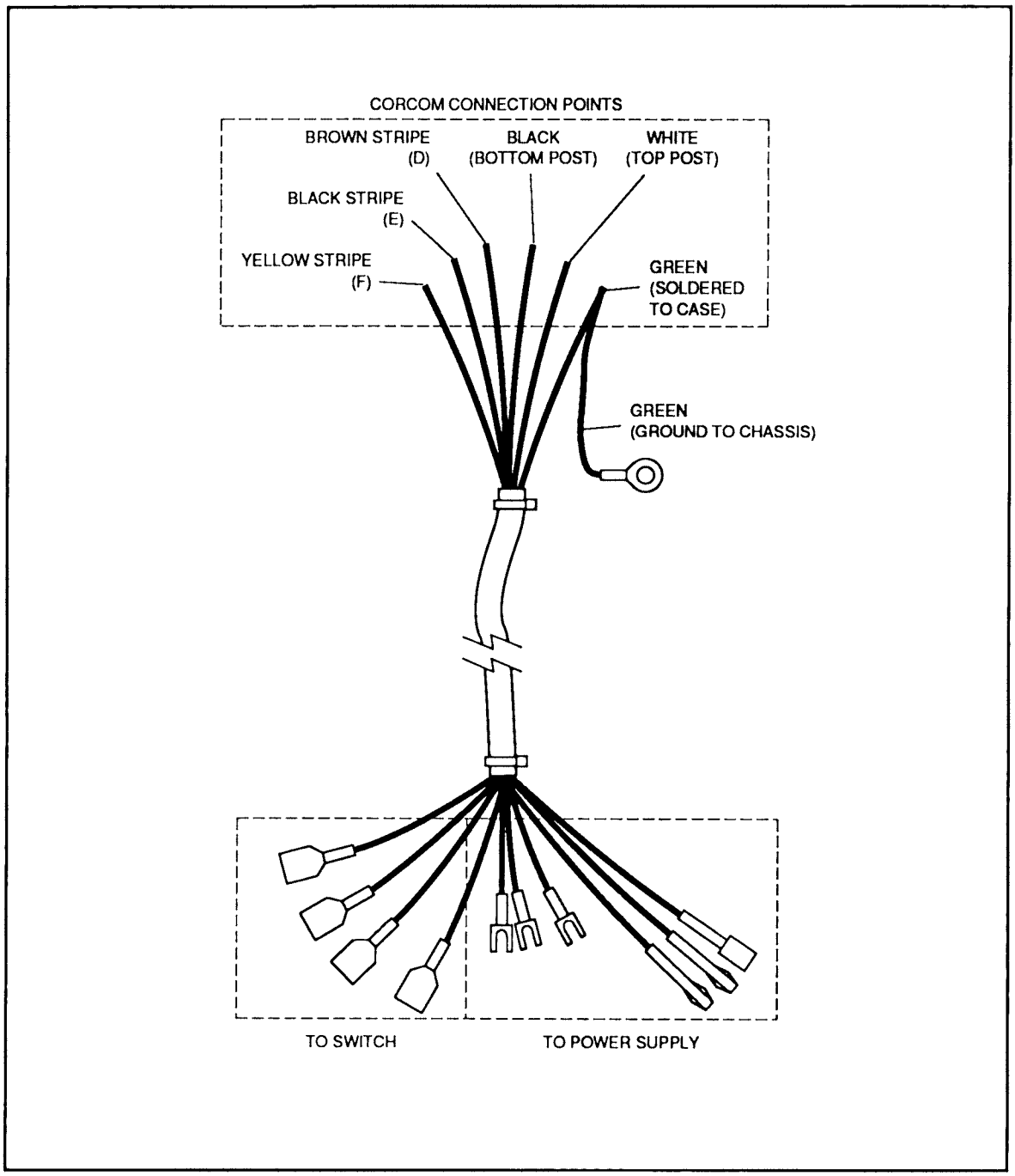


Figure 5-2. AC Harness

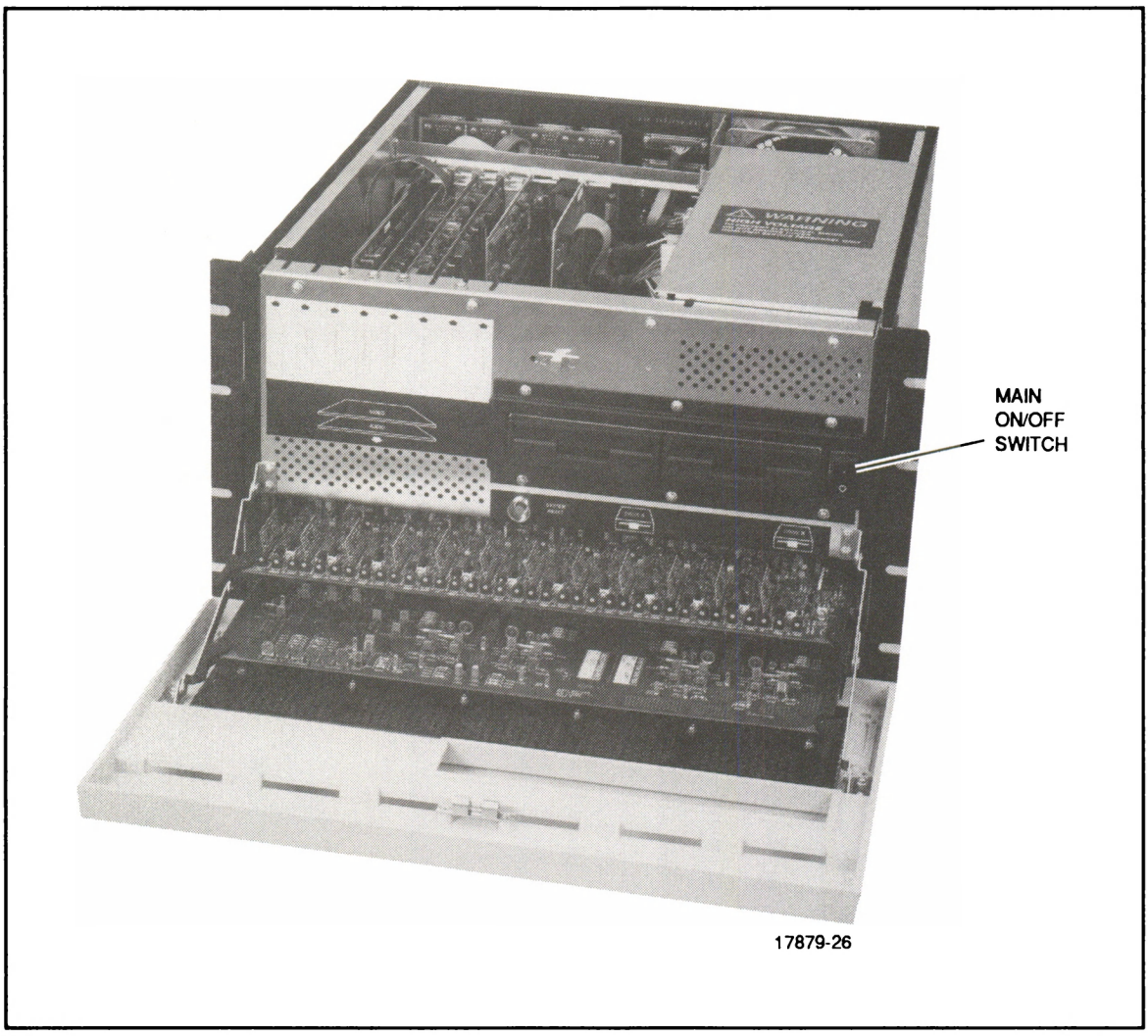


Figure 5-3. Main ON/OFF Switch for Edit Controller

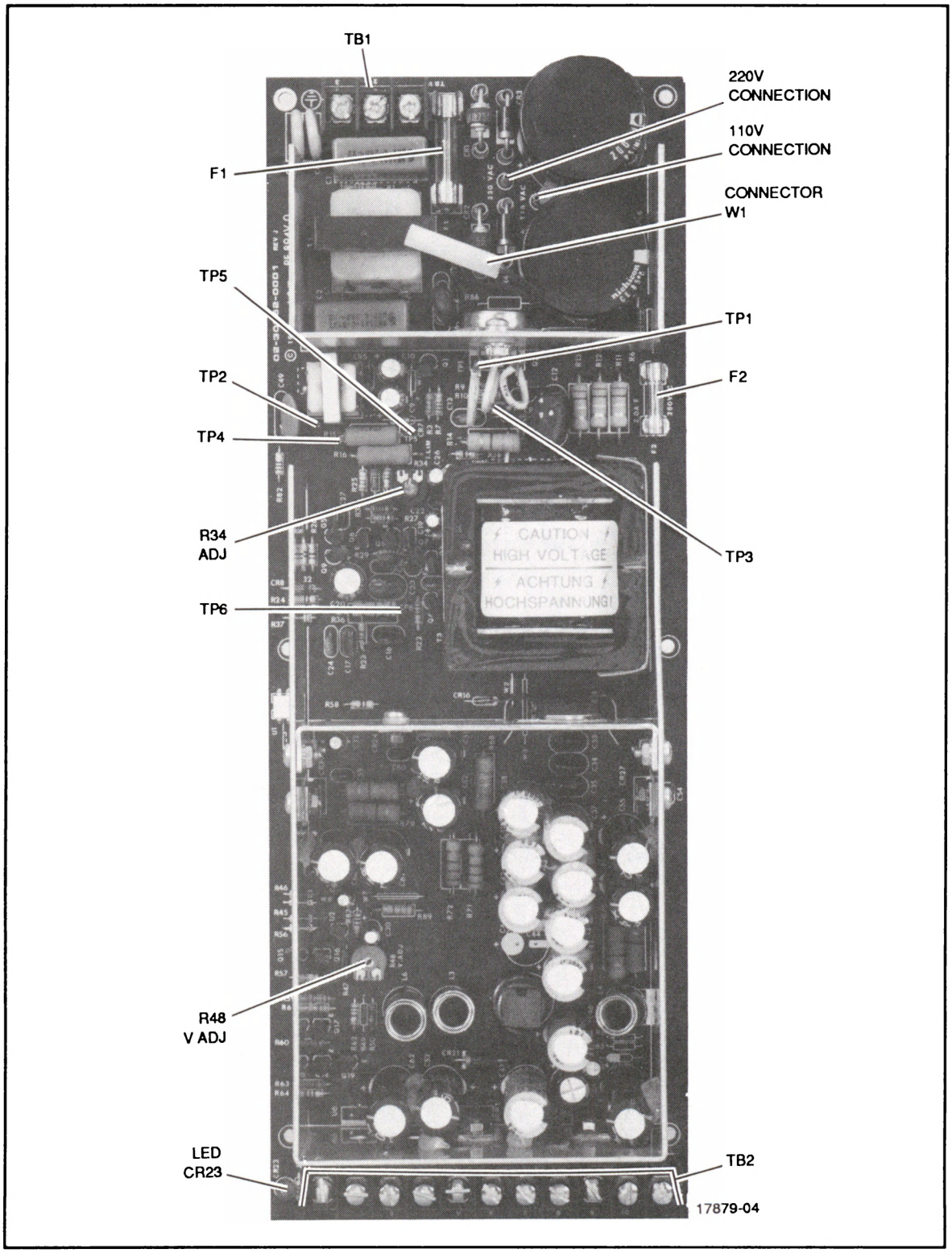


Figure 5-4. Edit Controller Power Supply (Condor Type)

Table 5-1. Power Supply Terminal Strip A Contacts

Contacts	Signal Description
Terminal Strip A	
1	AC in
2	AC Neutral
3	AC Ground
Terminal Strip B	
1	Logic In
2	Power Fail
3	+15V DC Out (5.0 Amp)
4	Out
5	+15V DC Out (
6	+5V DC Out (16.0 Amp)
7	Not Used
8	COIL
9	Not Used
10	–5V DC Out (0.6 Amp)
11	–15V DC Out (5.0 Amp)

5-11 POWER SUPPLY (SSI TYPE)

Newer ACE 25 systems use an SSI-type power supply, shown in Figure 5-5. Terminal strip connections are similar to those shown in Table 5-1. Adjust the power supply as follows:

Note

R40 (V4 ADJ) and R41 (V3 ADJ) are not used.

1. Attach voltmeter probe to pin 10 of U87 on the CPU Motherboard PWA.
2. Adjust R29 on power supply to achieve a +5.1V reading on the voltmeter (see Figure 5-5).
3. Disconnect voltmeter probe.

The SSI-type power supply has one fuse rated at 4.0 amp.

The Power Supply Replacement Kit (P/N 1431367) contains a power supply sub-assembly (P/N 1431369), consisting of a power supply mounted to a sheet metal adapter plate and ac select wires with attached connector, plus two cable harness assemblies. One harness connects the power supply to the Regulator PWA, and the other adapts the voltage select harness to the new power supply.

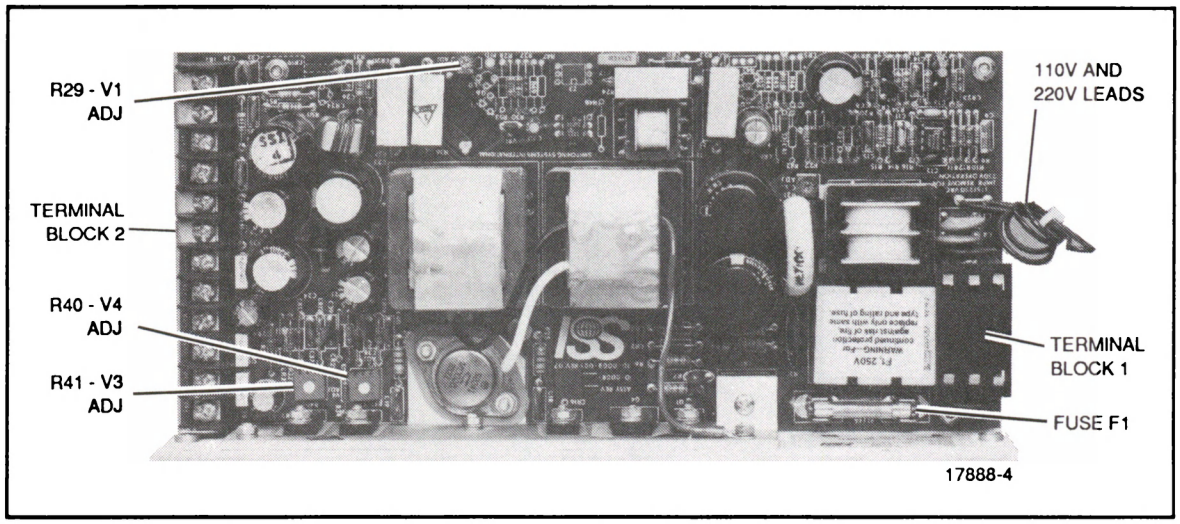


Figure 5-5. Edit Controller Power Supply (SSI Type)

To replace the power supply:

1. Remove old power supply (refer to paragraph 5-10).

2. Place the new SSI-type power supply on the mounting plate, hooking the sheet metal plate in the opening in the chassis sheet metal. Use three screws from old power supply to secure new power supply in place.

3. Connect ac wires to power supply terminal block 1. These wires are color-coded as follows:

   Line (Power): Black

   Neutral: White

   Ground: Green

4. Connect new ac select wires to existing ac harness and to connector from power supply. Match wire colors when connecting adapter.

5. Route dc harness through hole between Regulator PWA and power supply cage. The grommet may have to be loosened and refitted in the hole to route the harness.

6. Connect dc harness to Regulator PWA.

7. Carefully connect dc harness to power supply terminal block 2. All wires connect in order along terminal block.

8. Install ac line cord and turn power on to Edit Controller unit. Fan should operate.

9. Replace covers and re-attach all cables.

5-12 REGULATOR PWA

The Regulator PWA (P/N 1431446) regulates the various dc output voltages from the power supply, and produces -12V dc and +12V dc voltages These dc voltages are distributed to PWAs in the ACE 25. The power fail line from the power supply passes through the Regulator PWA to the CPU Motherboard PWA. Figure 5-6 shows the location of test points and connectors. Extra connectors on the board are not used; instead, PWAs draw power from the PC AT bus. There are no adjustments on the PWA that are performed outside of the factory.

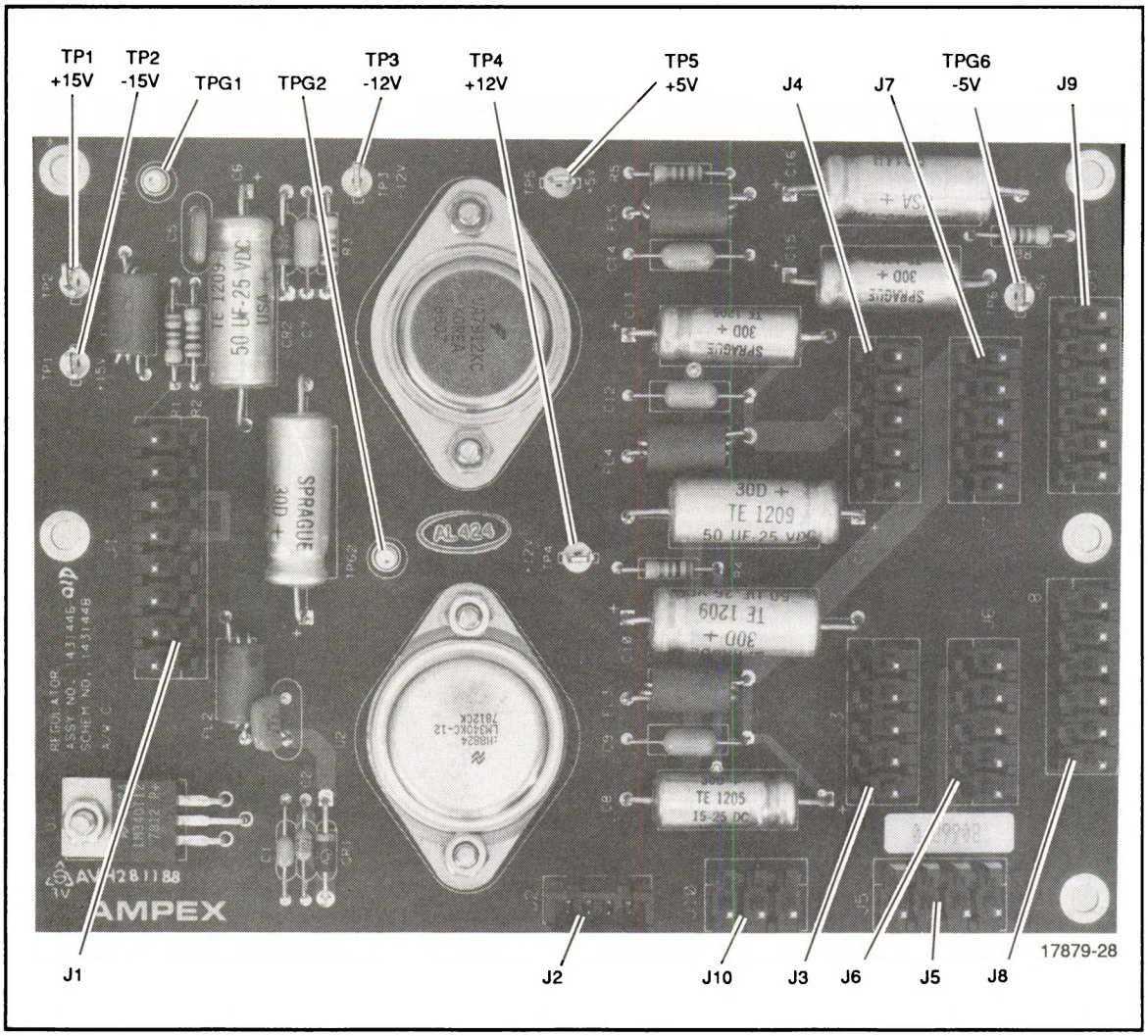


Figure 5-6. Regulator PWA

The +15 V and -15 V inputs are used to produce +12 V and -12 V, respectively. If +8 V is produced instead of +12 V, or -8 V instead of -12 V, verify that the input is actually +15 V/-15 V. A lower input voltage will produce a correspondingly lower output voltage.

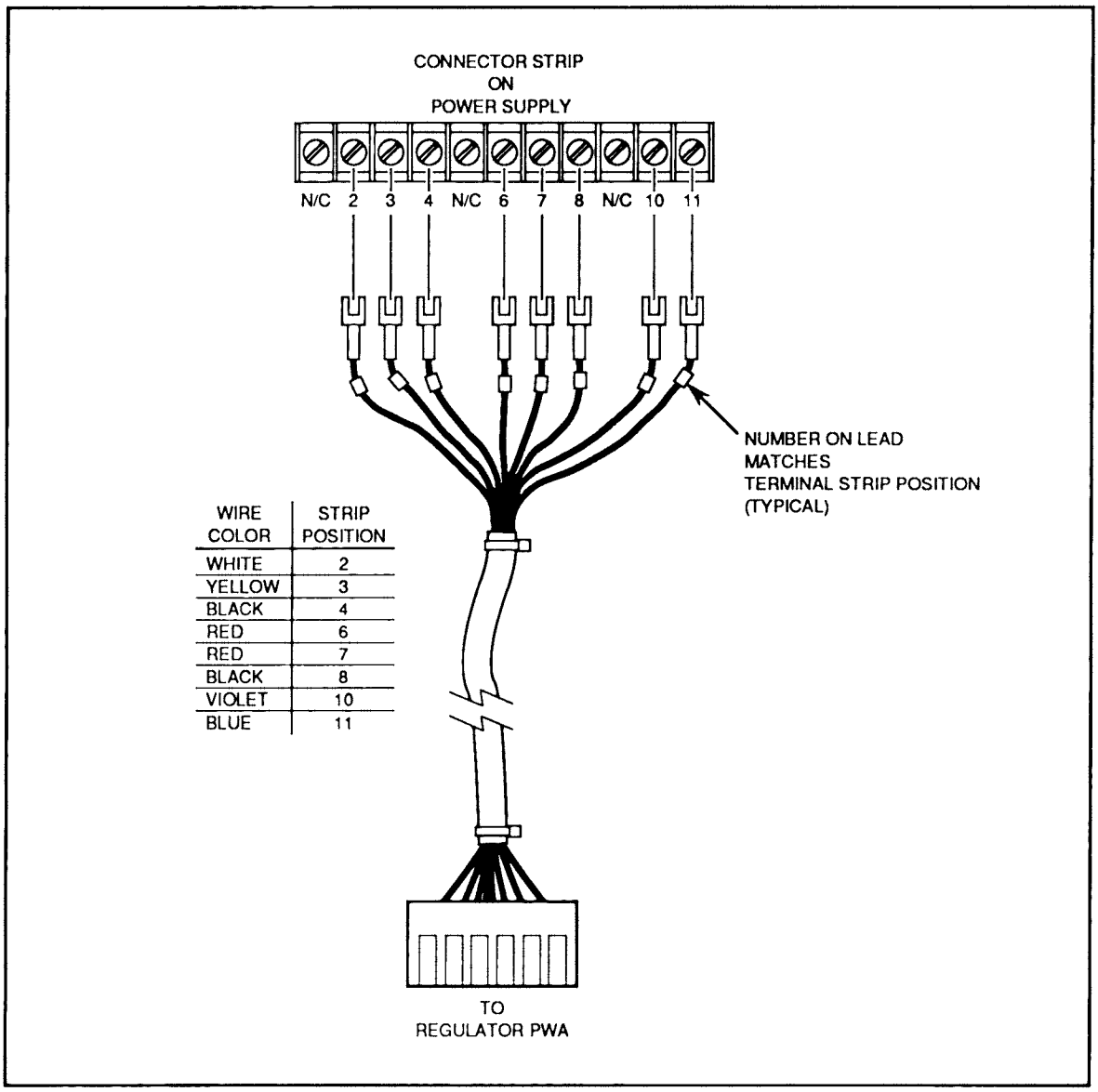
Table 5-2 lists the test points, and Table 5-3 lists the connectors . Leads on the Power Supply/Regulator PWA Harness (attached at connector J1), are identified in Figure 5-7.

Table 5-2. Regulator PWA Test Points

Test Point	Signal Description
TPG1	Digital Ground
TPG2	Analog Ground
TP1	+15Vdc
TP2	-15Vdc
TP3	-12Vdc
TP4	+12Vdc
TP5	+5Vdc
TP6	-5Vdc

Table 5-3. Regulator PWA Connections

Connector	Connects To	Connector Signals
J1	Power Supply Terminal Block B	Power Supply/Regulator PWA Harness
J2	Fan Harness	+12Vdc and Ground to Fan
J3	Not Used (Reserved for Switcher Backplane)	
J4	Not Used	
J5	Not Used	
J6	Not Used	
J7	Not Used	
J8	CPU Motherboard PWA Connector J5	Power Fail, +5V dc, +12Vdc, –12Vdc
J9	CPU Motherboard PWA	+5Vdc, –5Vdc
J10	Input/Output PWA Connector J16	+5Vdc



WIRE COLOR	STRIP POSITION
WHITE	2
YELLOW	3
BLACK	4
RED	6
RED	7
BLACK	8
VIOLET	10
BLUE	11

Figure 5-7. Power Supply Regulator PWA Harness

5-13 DC FAN

The dc fan is mounted inside the rear of the Edit Controller unit. Power is supplied via a harness connected to J2 on the Regulator PWA. The dc fan should be replaced as a complete unit if failure occurs. Figure 5-8 shows the dc fan mounted on the inside the the I/O Panel.

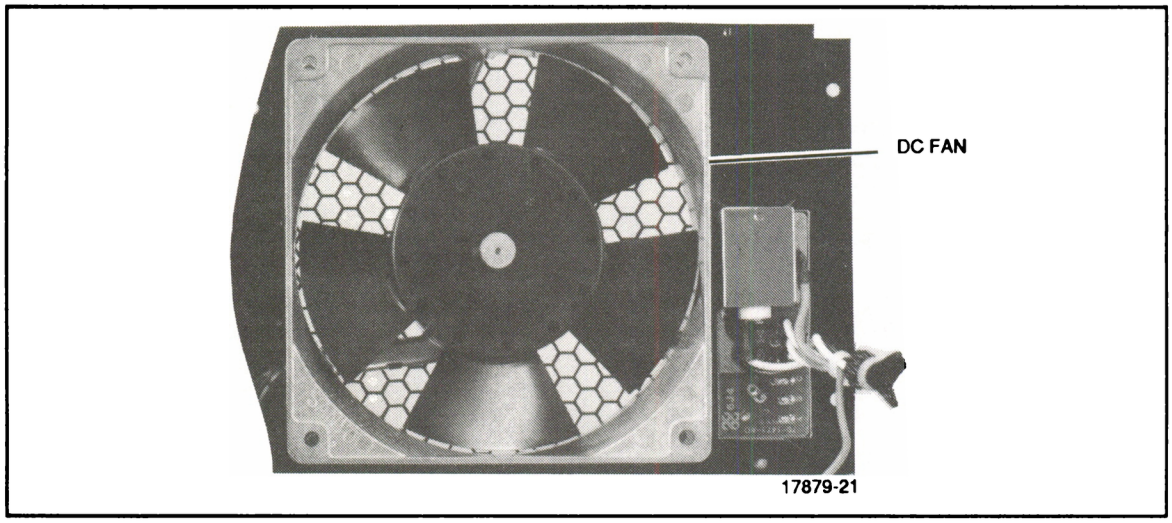


Figure 5-8. DC Fan

SECTION 6

CPU MOTHERBOARD PWA

6-1 GENERAL DESCRIPTION

The CPU Motherboard PWA (P/N 1431566) is a single-board computer fully compatible with the IBM AT personal computer. The central microprocessor on this board is an Intel 80286. The board has expansion slots for other system boards, plus two serial ports and one printer port. Figure 6-1 identifies the major items on the CPU Motherboard PWA.

6-2 PRIMARY BOARD COMPONENTS

The main components on the CPU Motherboard comprise:

80286 CPU (U80) – Main CPU for system (16-bit); runs at 10 MHz clock rate, with zero wait states; has 24 address bits capable of addressing up to 16 megabytes of memory.

82288 Bus Controller (U71) – Decodes CPU bus cycle states , memory, and I/O enables, to provide command and control outputs to AT bus.

82284 Clock Generator (U101) – Provides system clock signal, RESET, and READY signals to CPU. RESET signal is derived from Power-Good signal sent from power supply. READY signal indicates completion of a bus cycle.

8287 Programmable DMA Controllers (U137, U146) – Perform high-speed data transfers in memory and with I/O devices. One controller handles 8-bit data; the other is used for 16-bit data transfers.

8259 Programmable Interrupt Controllers (U140, U148) – Each IC provides eight levels of interrupt control. ACE 25 is an interrupt-driven system, with all I/O devices (such as keyboard or display monitor) communicating with the CPU via interrupts.

8042 Microprocessor (U129) – Custom chip functions as keyboard controller to decode input from the PC- (or AT-) style keyboard.

87128 PROMs (U18, U39) – PROMs (Programmable Read-Only Memory) contain BIOS (Basic Input/Output System), which controls all information exchange between CPU and I/O devices (except disk drives); also contain a self-test program which is run at power-up to detect faulty memory locations.

4257 RAM – One megabyte of RAM (Random Access Memory); consists of 36 chips (256 Kbytes -by-9) that are organized into Bank 0 and Bank 1, and operate as 8 bits of data and 1 bit of parity. RAM is socketed for replacement.

PC-AT Bus Slots – Eight slots in bus for expansion boards: six AT slots, and two PC slots.

6-3 SWITCH POSITIONS

Figure 6-2 shows the location of switches and their settings, on the CPU Motherboard PWA.

6-4 CONNECTORS

Figure 6-3 shows the location of connectors the the CPU Motherboard PWA. Table 6-1 lists the pin assignments for each connector.

6-5 THEORY OF OPERATION

Figure 6-4 is a block diagram showing the primary functions on the CPU Motherboard PWA, along with the routing of address, data and control signals.

6-6 80286 CPU

The 80286 microprocessor (U80) has a 24-bit address, 16-bit memory interface, an extensive instruction set, DMA and interrupt support capabilities, integrated memory management, 1-gigabyte of virtual address space for each task, and two operating modes. The ACE 25 uses the real address mode, in which the microprocessor's physical memory is a contiguous array of up to one megabyte.

1. RAM (RANDOM ACCESS MEMORY)
2. 27128 BIOS PROMS (U18/U39)
3. PC AT BUS SLOTS
4. 80286 CPU (U80)
5. 82284 CLOCK GENERATOR (U101)
6. 8042 MICROPROCESSOR (U129)
7. 8259 PROGRAMMABLE INTERRUPT CONTROLLERS (U140/U148)
8. 8237 PROGRAMMABLE DMA CONTROLLERS (U137/U146)
9. 82288 BUS CONTROLLER (U71)

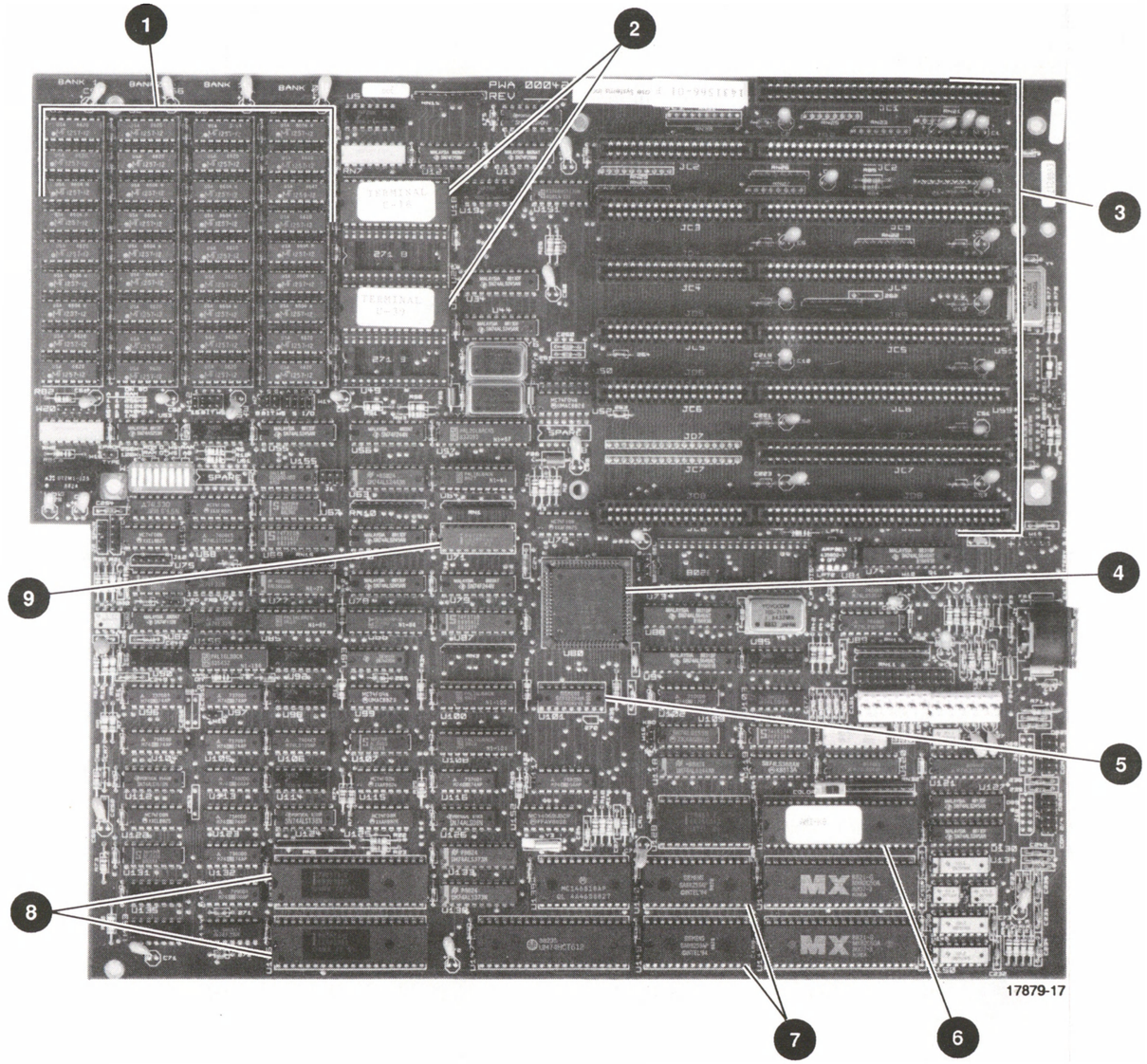


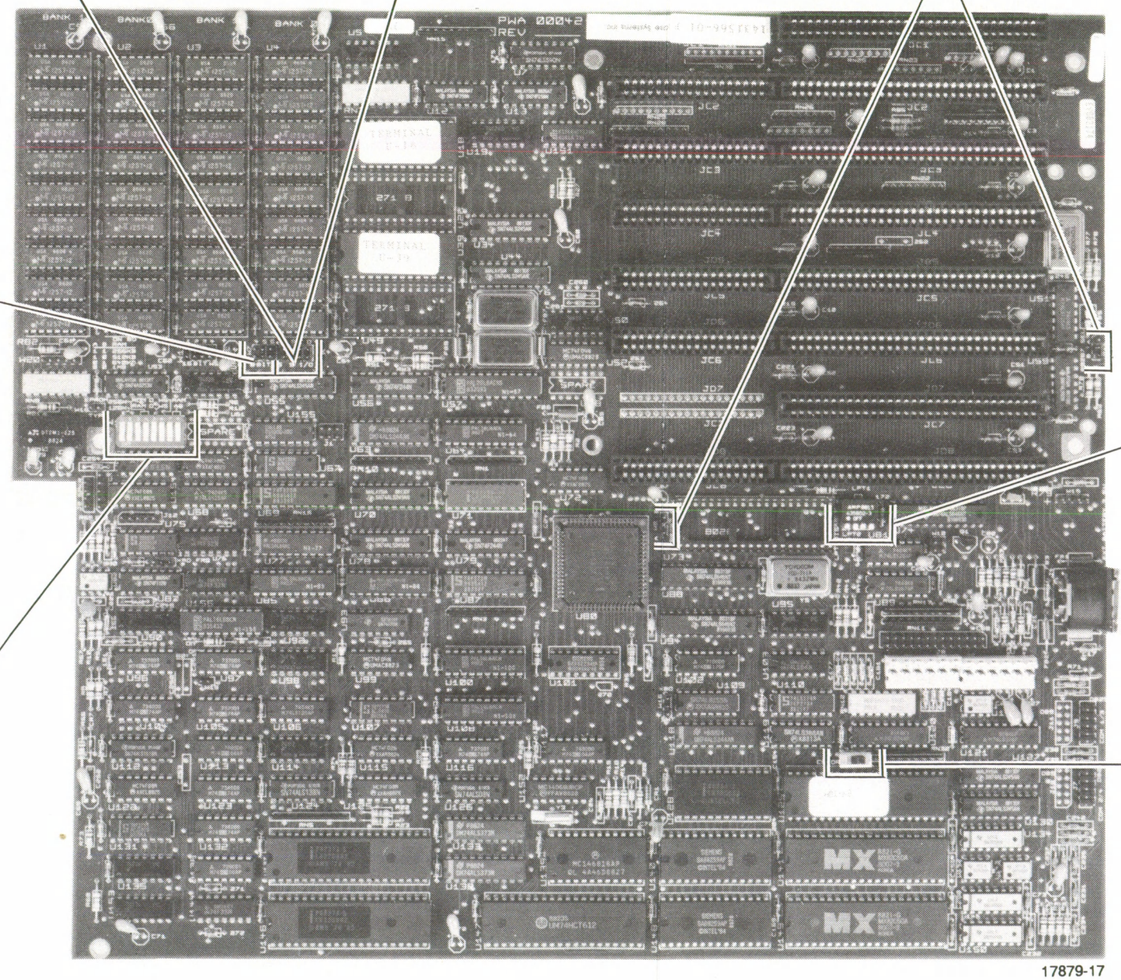
Figure 6-1.
CPU Motherboard PWA

Serial Port 1			
COM	IRO	W14A	W14B
1	4	ON	ON
3	4	ON	OFF
DIS	NONE	OFF	OFF

Serial Port 2			
COM	IRO	W14AC	W14D
2	3	ON	ON
3	3	ON	OFF
DIS	NONE	OFF	OFF

W8/W11 80287 Speed		
Speed	W8	W11
5 MHz	B	B
8 kMHz	A	A
10 MHz	A	B

W7 8–Bit Access Cycle Wait State Select	
Wait States	Jumper Setting
4	4
5	5
6	6



W4 Parallel Port Configuration					
LPT	S1	S2	S3	S4	IRQ
1	ON	OFF	ON	OFF	IRQ7
2	ON	ON	OFF	ON	IRQ5
DIS	OFF	OFF	OFF	OFF	NONE

W1 Memory Configuration		
Positions	Setting	Function
1 and 2 3 and 4	ON OFF	128K EPROM
1 and 2 3 and 4	OFF ON	256K EPROM
5	ON	0 Wait State
5	OFF	1 Wait State
6	OFF	Factory Setting
7 and 8	ON	256K RAM
7 8	ON OFF	512K RAM
7 8	OFF ON	640K RAM
7 and 8	OFF	1024K RAM

W3 Display Adaptor Type	
Switch Direction	Adaptor Card
→	Mono
←	Color

Figure 6-2.
CPU Motherboard PWA Switches

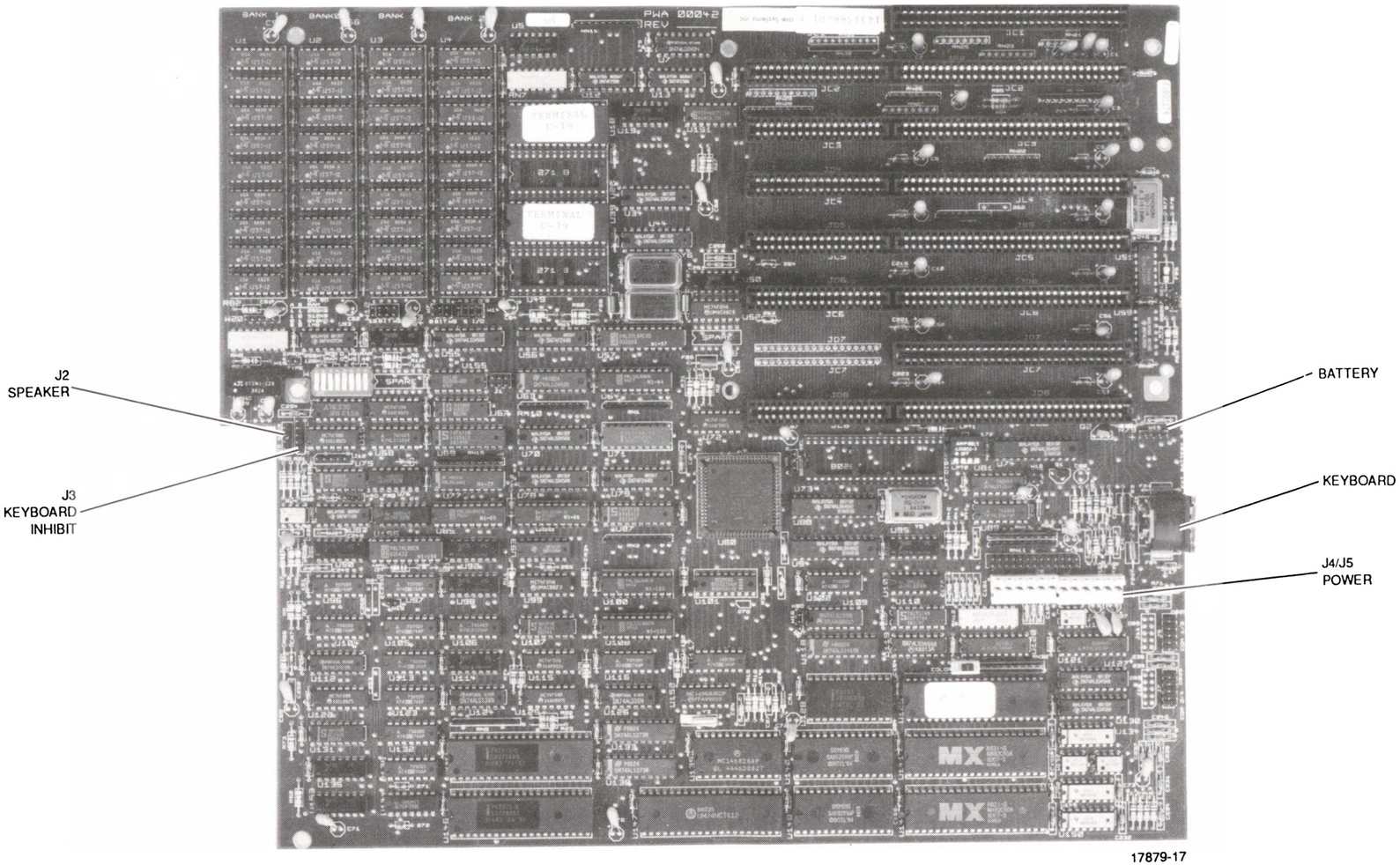


Figure 6-3.
CPU Motherboard PWA Connectors

Table 6-1. CPU Motherboard PWA Connector Pin Assignments

Pin	Assignment
J2 - Speaker Connector (4-Pin Header)	
1	Speaker
2	Key
3	High Speed
4	Vcc Indicator
J3 - Keyboard Inhibit Connector (5-Pin Header)	
1	Power on LED
2	N/C
3	Ground
4	Power Light +
5	Power Light -
J4 - Keyboard Connector (5 Pin Header)	
1	Clock
2	Data
3	N/C
4	Ground
5	Vcc
J12 - Power Good Signal (5-Pin Header)	
1	Turbo Light +
2	Turbo Light -
3	Reset
4	Ground
5	Turbo Speed

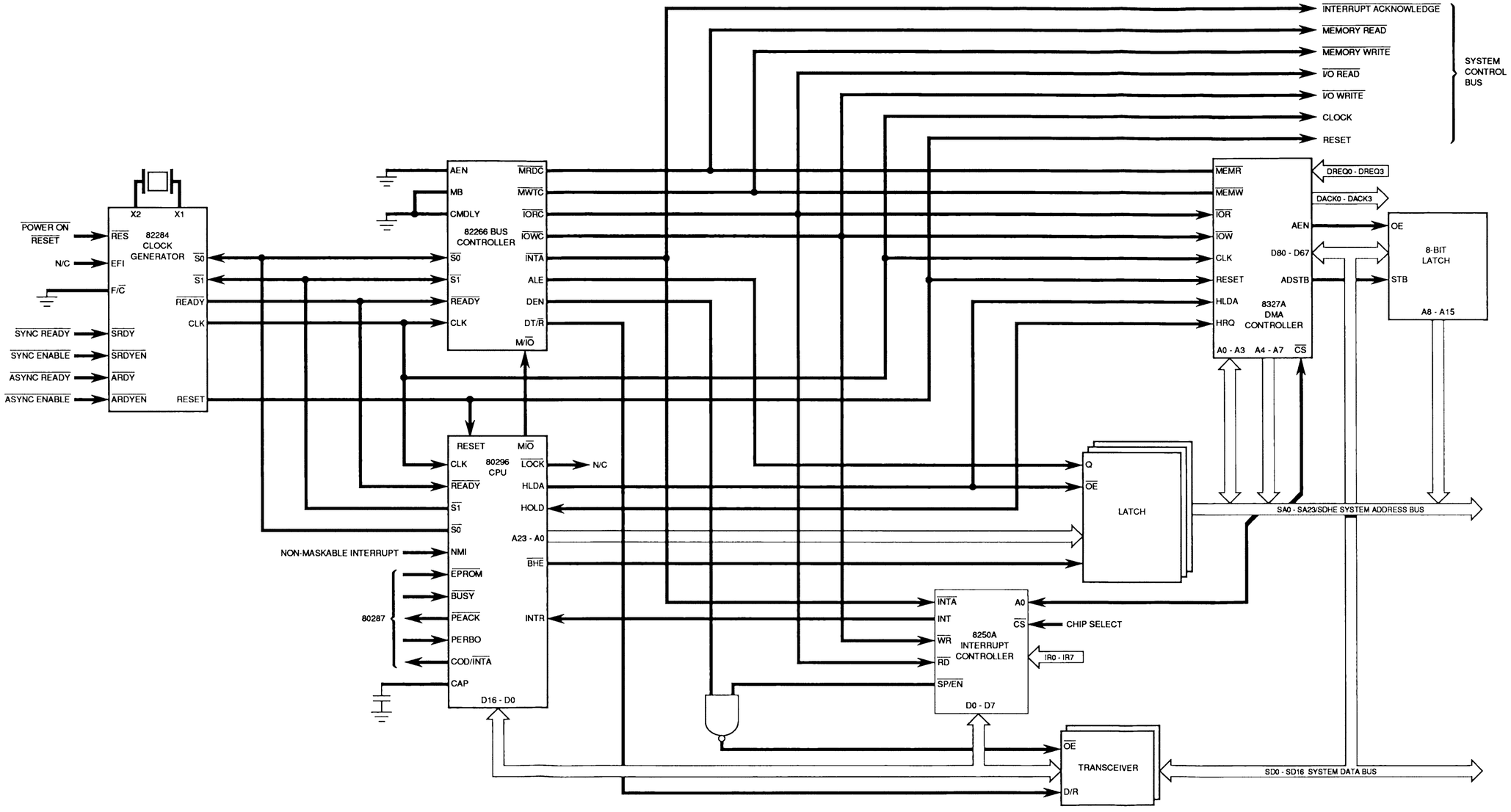


Figure 6-4.
CPU Motherboard PWA
Block Diagram

6-7 82284 Clock Generator

The role of the Clock Generator (U101) is to provide the CPU with a clock pulse (CLK) for system timing, and alert the CPU if delays are needed to lengthen bus cycles. The Clock Generator produces a CLK signal derived from the oscillator (Y6/Y7), and must have a Power Good signal from the power supply.

The CLK, RDY and RES signals are sent from the Clock Generator to the CPU. Two ready inputs are used to develop the -RDY outputs: Synchronous Ready and Asynchronous Ready. The -SRDY signal is used to length the memory access cycle, while the -ARDY signal stretches bus cycles. The PC/AT expansion bus signal I/O CH RDY is connected to the 82284's -ARDY line, and is pulled low by slow devices. The ILC PWA uses the I/O CH RDY signal to delay memory read/write to the shared RAM (on the ILC PWA) while the RAM is being accessed by the ILC's CPU.

6-8 Wait State Logic

The wait state logic determines if extra clock cycles are needed to complete operations. When the CPU's -READY line is pulled low, extra clock cycles are added to the machine cycle (known as wait states). During a wait state, the CPU monitors -READY to see if it goes high, then resumes operation.

6-9 82288 Bus Controller

The 82288 bus controller (U71) decodes three signals (M/-IO, -S1, -S0) from the CPU to provide command and control outputs to the system bus. Bus cycles from the CPU are in three forms: Read, Write, and Halt. Read cycles include interrupt acknowledge, memory, and I/O read. Write cycles are memory and I/O write. Halt bus cycles differ from read and write cycles in that no command or control output is activated. All control inputs are ignored until the next bus cycle is started by changes in S1 and S0.

The 82288 outputs five command signals (MEMRD, MEMWR, I/O RD, I/O WR, and IACK), and provides three control signals (Address Latch Enable, Data Enable and Data Transport/-Receive). Control signals are used to set up data/address buffers on the system bus.

Command timing can be altered using the CMDLY signal to set command start time and the READY signal to set end time. In the ACE 25, CMDLY is used to set various memory read/write start timings.

6-10 8259A Interrupt Controller

The two 8259A Interrupt Controller chips (U140 and U148) manage interrupts to the CPU. The interrupt sequence is as follows:

- A peripheral device raises one or more Interrupt Request lines (IR7-IR0) high.
- The Interrupt Controller evaluates requests and sends INT signal to the CPU, according to the interrupt level and if the interrupt has not been masked by the CPU.
- The CPU acknowledges the interrupt by setting signals M/-IO, -S1 and -S0 low. The bus cotroller decodes these lines and pulls -INTA low.

- When the Interrupt Controller receives the -INTA pulse, the Controller sets the highest priority bit of its internal Interrupt Register and resets the corresponding Interrupt Request Register.
- The CPU then initiates a second -INTA pulse. While this pulse is active, the interrupt controller places an 8-bit vector pointer address on the data bus, where it is read by the CPU. This vector address is the location of the operational outline for the device that generated the interrupt.

The remaining four inputs to the interrupt controller (-WR, -RD, A0 and -CS) are used when the CPU needs to write setup commands or read the status of the interrupt controller.

6-11 8237A Direct Memory Access Controller

The Direct Memory Access (DMA) Controller (U137 and U146) allow external devices to directly transfer information to and from system memory. ACE 25 has two DMA controllers which are cascaded. Each 8237A chip has four independent DMA channels. Using 16-bit addressing, the controller can transfer up to 64 Kbytes of memory.

An external 8-bit latch is used to hold the upper address byte which appears on the controller's data lines. Since transfers are sequential, the upper address byte changes only once every 256 bytes during the transfer.

Before a transfer starts, the BASE (starting) address and COUNT (number of bytes to transfer) are sent to the DMA channel by the CPU. This information initializes the controller's Current Address and Count registers, which are decremented after each byte is transferred.

When an I/O device wants to transfer data, it enables its DREQ (DMA Request) line. The DMA controller then issues a hold request (HRQ) to the CPU to gain control of the bus. The CPU floats its bus drivers to tri-state off and issues a hold acknowledge (HLDA) to the DMA Controller. This causes the controller to signal the I/O device via the DACK (DMA Acknowledge) strobe to place a byte onto the data bus. At the same time, the controller supplies a memory address and signals the data destination to read the byte.

For I/O-to-memory transfers, -MEMW, -IOR, and DACK become active at the same time. For memory-to-I/O transfers, the -MEMR, -IOW, and DACK lines are active at the same time.

The DMA process uses five clock cycles for a transfer, compared to 29 cycles for a CPU-controlled transfer.

6-12 I/O Channel

The I/O Channel is used to connect peripheral devices in the PC/AT bus slot with the main CPU. Figure 6-5 shows the location and numbering of the I/O channel connectors. These connectors consist of eight 62-pin and six 36-pin edge connector sockets. Figure 6-6 shows the pin numbering and pin signals for these connectors. Table 6-2 describes these pin signals.

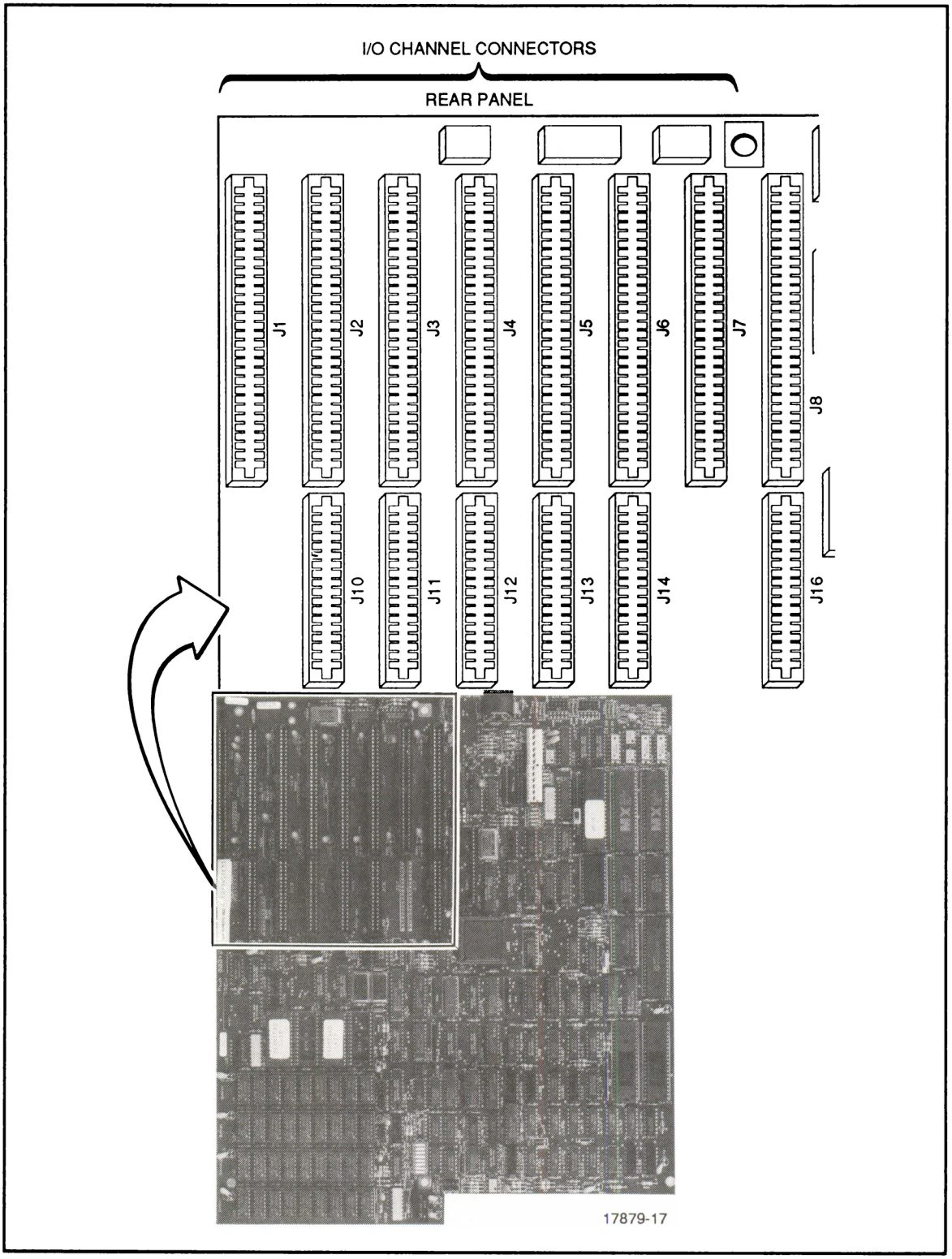


Figure 6-5. CPU Motherboard PWA I/O Channel Bus Connectors

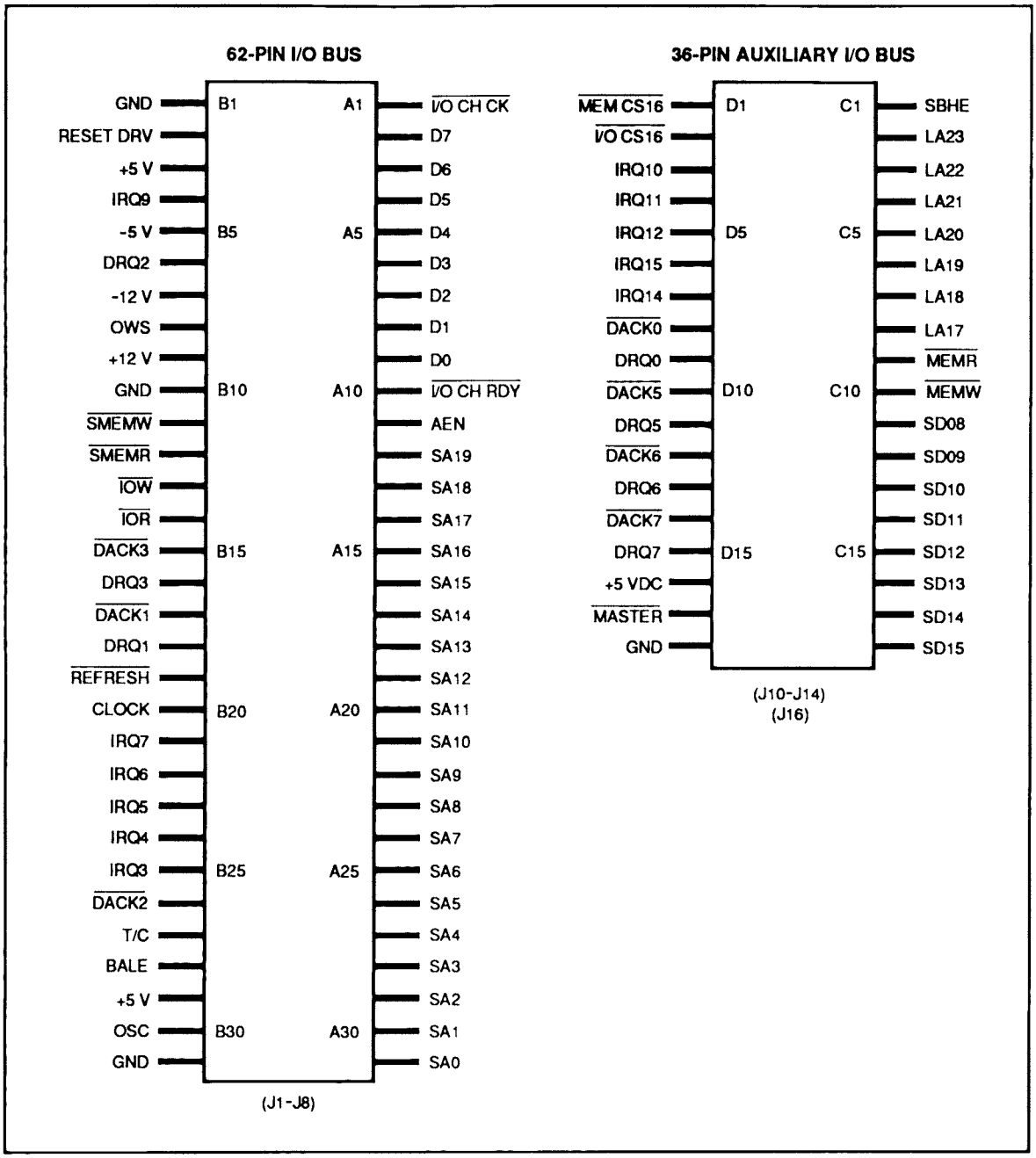


Figure 6-6. I/O Channel Bus Connectors Pin Signals

Table 6-2. Input/Output Channel Bus Pin Assignments

Pin	Signal	I/O	Description
62 - Pin Input/Output Bus			
A1	–I/O CH CK	I	Parity Error Check – System Error
A2	D7	I/O	Data Bit 7
A3	D6	I/O	Data Bit 6
A4	D5	I/O	Data Bit 5
A5	D4	I/O	Data Bit 4
A6	D3	I/O	Data Bit 3
A7	D2	I/O	Data Bit 2
A8	D1	I/O	Data Bit 1
A9	D0	I/O	Data Bit 0
A10	–I/O CH READY	I	Add Wait State to Memory or I/O Cycle
A11	AEN	O	Enables 16-bit DMA Address Bus
A12	SA19	I/O	System Address Bit 19
A13	SA18	I/O	System Address Bit 18
A14	SA17	I/O	System Address Bit 17
A15	SA16	I/O	System Address Bit 16
A16	SA15	I/O	System Address Bit 15
A17	SA14	I/O	System Address Bit 14
A18	SA13	I/O	System Address Bit 13
A19	SA12	I/O	System Address Bit 12
A20	SA11	I/O	System Address Bit 11
A21	SA10	I/O	System Address Bit 10
A22	SA9	I/O	System Address Bit 9
A23	SA8	I/O	System Address Bit 8
A24	SA7	I/O	System Address Bit 7
A25	SA6	I/O	System Address Bit 6
A26	SA5	I/O	System Address Bit 5
A27	SA4	I/O	System Address Bit 4

(Continued next page)

Table 6-2. Input/Output Channel Bus Pin Assignments (Continued)

Pin	Signal	I/O	Description
62 - Pin Input/Output Bus (Continued)			
A28	SA3	I/O	System Address Bit 3
A29	SA2	I/O	System Address Bit 2
A30	SA1	I/O	System Address Bit 1
A31	SA0	I/O	System Address Bit 0
B1	GND	G	System Ground
B2	RESET DRV	0	Resets System at Power-Up
B3	+5V	P	+5V Power
B4	IRQ9	I	UART Interrupt, redirected to IRQ2 (INT 0AH)
B5	-5V	P	-5V Power
B6	DRQ2	I	8-Bit DMA Interrupt
B7	-12V	P	-12V Power
B8	0WS	I	Zero Wait State
B9	+12V	P	+12V Power
B10	GND	G	Ground
B11	-SMEMW	O	Write to Lower 1 Megabyte of Memory
B12	-SMEMR	O	Read/Write Memory - Active in lower Memory
B13	-IOW	I/O	I/O Device Write
B14	-IOR	I/O	I/O Device Read
B15	-DACK3	O	DMA Request Acknowledge
B16	DRQ3	I	8-Bit DMA
B17	-DACK1	O	DMA Request Acknowledge
B18	DRQ1	I	8-Bit DMA
B19	-REFRESH	I/O	Activates Refresh Cycle
B20	CLOCK	O	System Clock
B21	IRQ7	I	Parallel Port 1

(Continued next page)

Table 6-2. Input/Output Channel Bus Pin Assignments (Continued)

Pin	Signal	I/O	Description
62 - Pin Input/Output Bus (Continued)			
B22	IRQ6	I	Disk Controller
B23	IRQ5	I	Parallel Port 2
B24	IRQ4	I	Serial Port 1
B25	IRQ3	I	Serial Port 2
B26	-DACK2	O	DMA Request Acknowledge
B27	T/C	O	DMA Terminal Count
B28	BALE	O	Address Latch Enable (For A0-A19)
B29	+5V	P	+5V Power
B30	OSC	O	14.31818 MHz Oscillator (70-nanosecond)
B31	GND	G	Ground
36 - Pin Input/Output Bus			
C1	SBHE	I/O	Bus High Enable (SD8-SD15)
C2	LA23	I/O	Address Bit 23 for Memory and I/O Devices
C3	LA22	I/O	Address Bit 22 for Memory and I/O Devices
C4	LA21	I/O	Address Bit 21 for Memory and I/O Devices
C5	LA20	I/O	Address Bit 20 for Memory and I/O Devices
C6	LA19	I/O	Address Bit 19 for Memory and I/O Devices
C7	LA18	I/O	Address Bit 18 for Memory and I/O Devices
C8	LA17	I/O	Address Bit 17 for Memory and I/O Devices
C9	-MEMR	I/O	Drives Data onto Data Bus to be Read
C10	-MEMW	I/O	Instructs I/O Devices to Store Data on Data Bus

(Continued next page)

Table 6-2. Input/Output Channel Bus Pin Assignments (Continued)

Pin	Signal	I/O	Description
36 - Pin Input/Output Bus (Continued)			
C11	SD08	I/O	Bus Bit 08 for CPU Memory or I/O Devices
C12	SD09	I/O	Bus Bit 09 for CPU Memory or I/O Devices
C13	SD10	I/O	Bus Bit 10 for CPU Memory or I/O Devices
C14	SD11	I/O	Bus Bit 11 for CPU Memory or I/O Devices
C15	SD12	I/O	Bus Bit 12 for CPU Memory or I/O Devices
C16	SD13	I/O	Bus Bit 13 for CPU Memory or I/O Devices
C17	SD14	I/O	Bus Bit 14 for CPU Memory or I/O Devices
C18	SD15	I/O	Bus Bit 15 for CPU Memory or I/O Devices
D1	-MEM CS16	I	16-Bit Data Transfer with 1 Wait State
D2	-I/O CS16	I	16-Bit I/O Cycle with 1 Wait State
D3	IRQ10	I	Reserved
D4	IRQ11	I	Reserved
D5	IRQ12	I	Reserved
D6	IRQ15	I	Reserved
D7	IRQ14	I	Hard Disk Interrupt
D8	-DACK0	O	DMA Request Acknowledge
D9	DRQ0	I	8-Bit DMA
D10	-DACK5	O	DMA Request Acknowledge
D11	DRQ6	I	16-Bit DMA
D12	-DACK6	O	DMA Request Acknowledge
D13	DRQ6	I	16-Bit DMA
D14	-DACK7	O	DMA Request Acknowledge
D15	DRQ7	I	16-Bit DMA
D16	+5V	P	+5V Power

6-13 Bus Structure

Figure 6-7 shows a block diagram of the bus structure on the CPU Motherboard PWA. The buses can be divided into three types: system control, address and data.

The system control bus has the control signals such as ALE (address latch enable), the read/write enables (IOR, IOW, MEMR, etc.), interrupts, and acknowledge signals.

The address and data buses are buffered to provide supplemental buses. The CPU A0-A19 Address Bus is buffered to provide the main System Address bus. The upper seven address bits (A17-A23) are buffered to provide the Local Address lines to the I/O Channel. Local Address bits are decoded on I/O cards to select the card's particular address range within the AT's 16-Mbyte memory. System Address bus bits SA0-SA16 are further buffered to provide an Extended Address bus, which addresses ROM and I/O circuitry on the motherboard. System Address bits SA1-SA16 are multiplexed to provide an 8-bit Memory Address bus for the RAM memory.

The CPU's 16-bit Data Bus is buffered to provide a System Data bus to the I/O Channel. The 16 System Data bus bits are further buffered as Memory Data bits MD0-MD15. These bits act as data to and from RAM and ROM on the system board. The lower 8 bits of System Data bus (XD0-XD7) are buffered to provide an Extended Data bus to all the I/O circuitry on the system board.

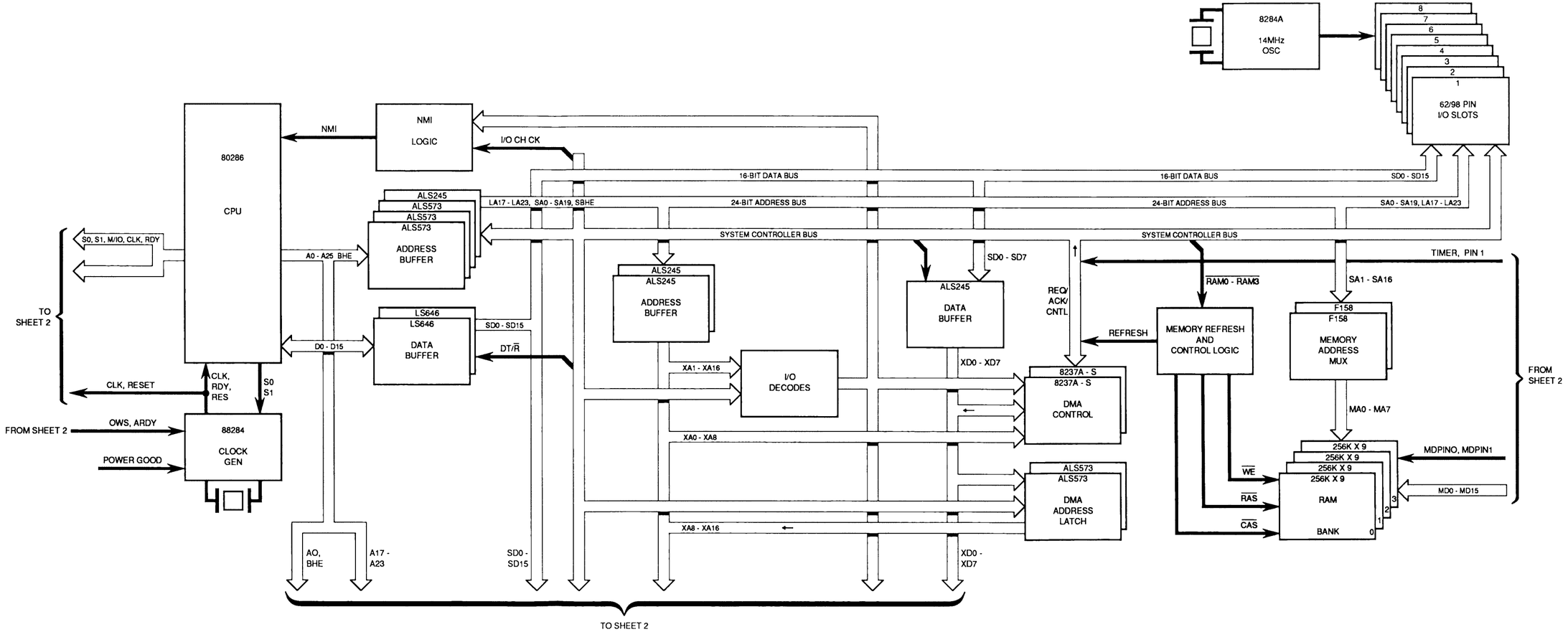


Figure 6-7.
CPU Motherboard PWA Bus Structure Block Diagram (Sheet 1 of 2)

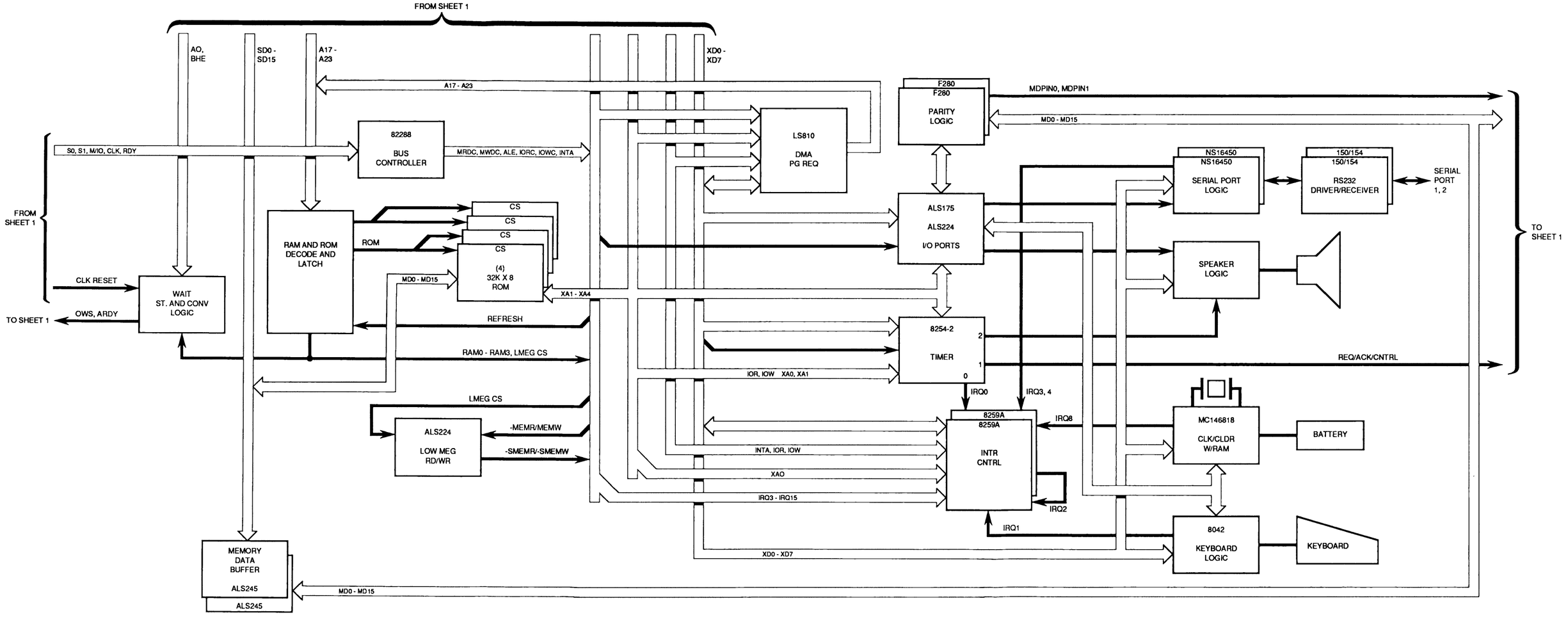


Figure 6-7.
CPU Motherboard PWA Bus Structure Block Diagram
(Sheet 2 of 2)

6-14 Power Good

The Power Good signal is generated in the power supply to indicate proper operation of the supply. This signal has a delay of 100 to 500 ms, and generates a high true System Reset on the Clock Generator's -RES input. It is TTL high for normal operation and low for fault condition. This signal is generated by ANDing the dc Output Voltage Sense and the ac Input Voltage Sense lines in the power supply. The dc Output Voltage Sense line holds the Power Good signal low until all output voltages have reached minimum levels. The ac signal causes the Power Good signal to go low at least 1 ms before any output voltage falls below limit.

6-15 Memory

The ACE 25 has 1 Mbyte of CMOS RAM memory and 256 Kbytes of system ROM memory. This memory is mapped as shown in Table 6-3.

The 1 Mbyte of RAM on the motherboard is comprised of 36 256K-by-1 RAM chips. There are two 512K-by-9 memory banks: Bank 0 and Bank 1. The ninth bit is for parity. There are two 74F280 Parity Generator/Checker chips—one for each RAM memory bank. Every time a byte of data is written to RAM, a bit is generated by the 74280. If the byte contains an even number of one's, the 74280's Even Parity Output pin is high. The result of the parity generation is stored as the ninth bit at the RAM address accessed. When data is read back from RAM, it's parity is checked again and compared with the stored bit.

The resultant signal, PCK (Parity Check) is used along with a similar I/O CH CK from the expansion slots to produce the PC/AT's Non-Maskable Interrupt (NMI). A difference between the parity bit written to RAM and that computed when the data was read back would indicate that the RAM data had been corrupted in some way. If either PCK or I/O CH CK are low, indicating a parity error, the generated NMI would cause the system to display a "Parity Check" error message and halt operation.

Table 6-3. CPU Memory Map

Address Location	Name	Description
000000 to 09FFFF	System RAM (640 Kbyte)	Duplicates IBM AT 512 Kbyte system memory plus 128 Kbyte Memory Expansion Board
100000 to 0AFFFF	Upper System RAM (384 Kbyte)	Upper portion of system RAM, located in I/O Channel memory space
FF0000 to FFFFFF	System ROM (64 Kbyte)	BIOS system software, duplicated at address 0F0000
FE0000 to FEFFFF	Extended System ROM (64 Kbyte)	Additional operating system software, duplicated at address 0E0000
0C0000 to 0DFFFF	Additional System ROM (128 Kbyte)	Located in I/O Channel ROM memory space
800000 to 80FFFF	8-Channel ILC Shared RAM (64 Kbyte)	Located in I/O Channel memory space at address 10000 to address FDFFFF

SECTION 7

DISK DRIVES, DISK DRIVE CONTROLLER PWA, AND MONOCHROME VIDEO DISPLAY ADAPTER PWA

7-1 INTRODUCTION

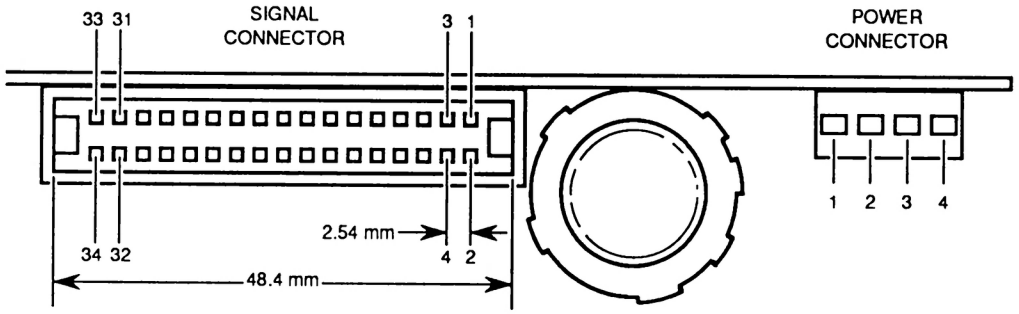
This section covers replacement of the Disk Drives, the Disk Drive Controller PWA, and the Monochrome Video Display Adapter PWA.

7-2 DISK DRIVES

The ACE 25 has two 3.5-inch floppy disk drives (P/N 1431582), designated as Drive 0 and Drive 1. These drives are not designed to be field-repairable, and should be replaced as a complete drive unit. Replacement part is Sony model MD-F73W-01D or equivalent. Each drive has a power and a signal connector, as shown in Figure 7-1, located on the rear of the drive. Table 7-1 lists the power signals, and Table 7-2 lists the control and data signals. A Drive Select switch (located on the right side near the rear (see Figure 7-2) is used to designate the drive assignment. If the drive is replaced, this switch must be set correctly, and the proper power and signal connectors attached to the new drive.

7-3 DISK DRIVE CONTROLLER PWA

The Disk Drive Controller PWA is a printed circuit board supplied by outside vendors. Individual boards may have minor differences from the PWA described in the following paragraphs. These differences do not affect the operation of the system.



DETAIL A

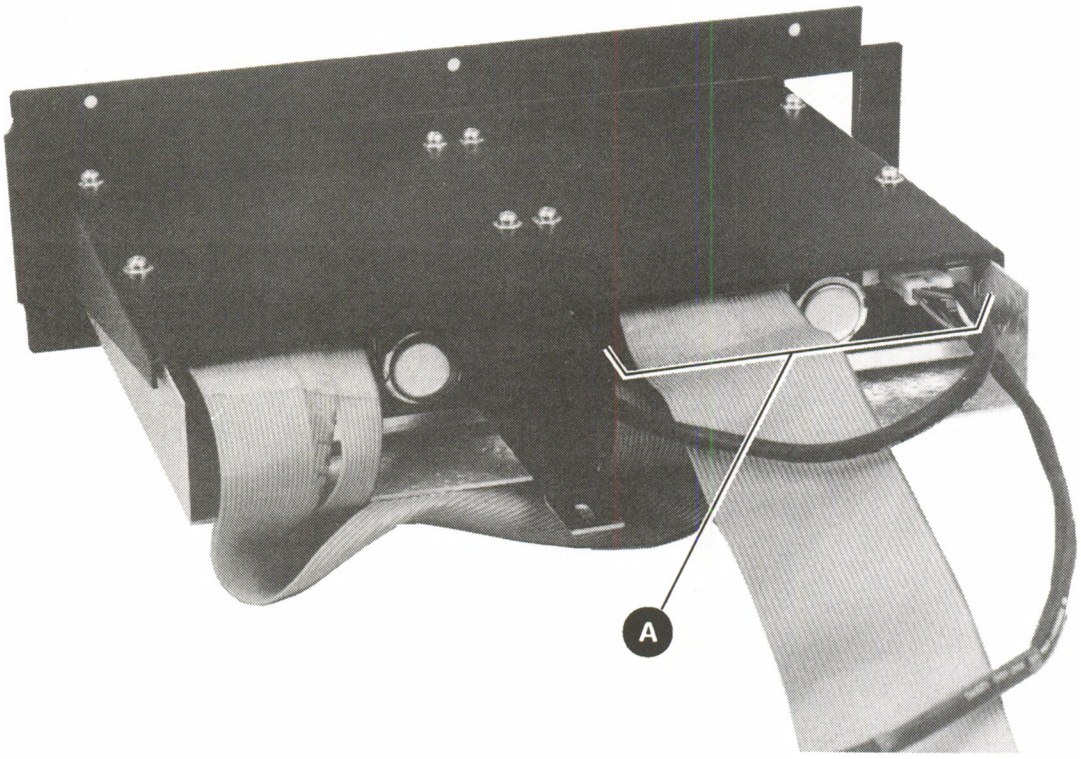


Figure 7-1. Disk Drive Connectors (Rear of Disk Drive)

Table 7-1. Disk Drive Power Signals

Pin	Signal Description
1	+5 Vdc Power
2	Ground (+5 Vdc Return)
3	Ground (+12 Vdc Return)
4	+12 Vdc Power
Note: Receptacle is AMP 171822-4 or equivalent, contacts are AMP 170262-1 or equivalent, and wires are AWG20.	

Table 7-2. Disk Drive Control and Data Signals

Pin	Signal Description	Pin	Signal Description
1	Return	18	Direction
2	N.C.	19	Return
3	Return	20	Step
4	N.C.	21	Return
5	Return	22	Write Data
6	Drive Select 3	23	Return
7	Return	24	Write Gate
8	Index	25	Return
9	Return	26	Track 00
10	Drive Select 0	27	Return
11	Return	28	Write Protocol
12	Drive Select 1	29	Return
13	Return	30	Read Data
14	Drive Select 2	31	Return
15	Return	32	Head Select
16	Motor On	33	Return
17	Return	34	Disk Change
Note: Receptacle is 3M 3414-6500xx or equivalent, and cable is 3M 3365/34 or equivalent.			

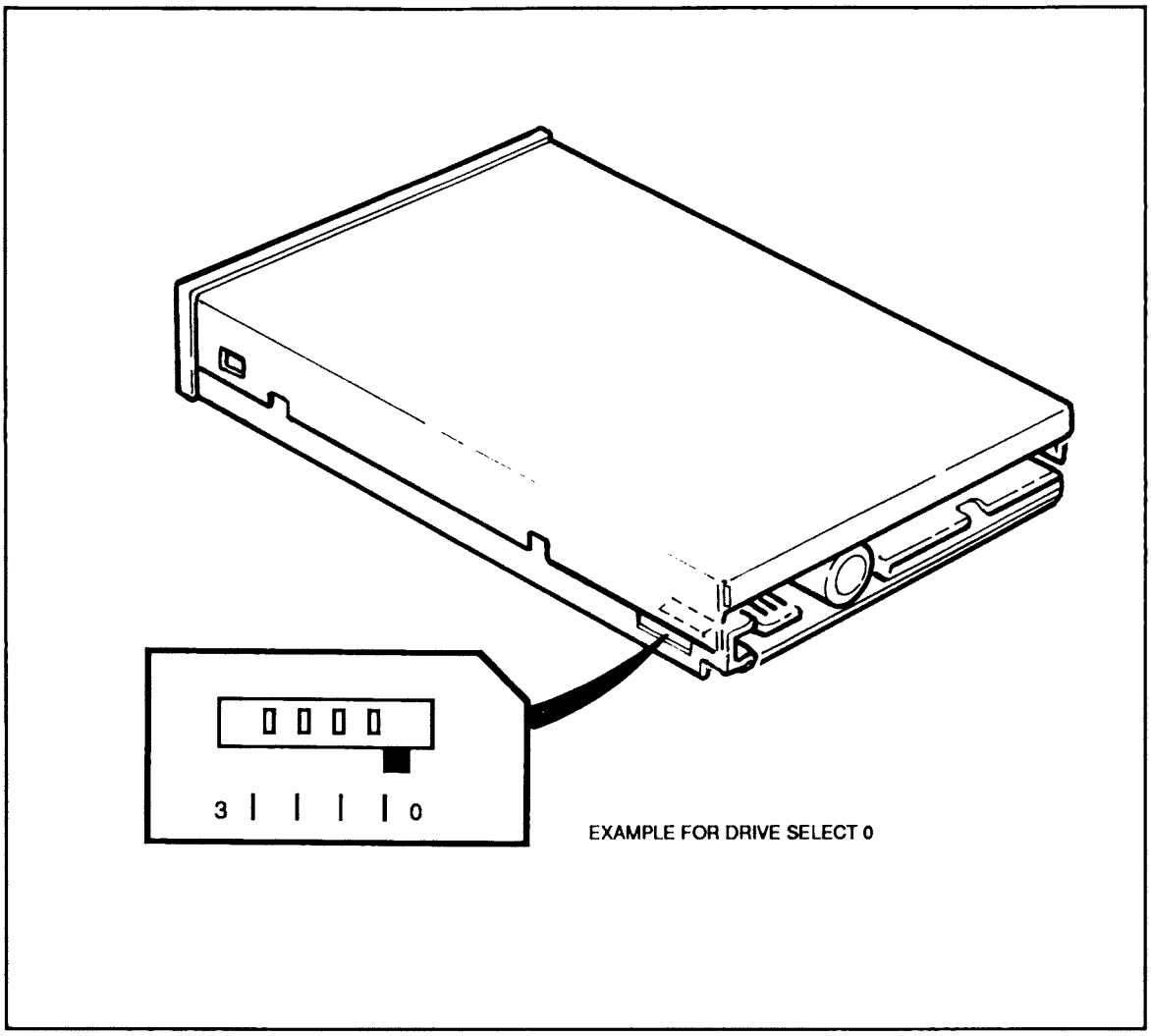


Figure 7-2. Drive Select Switch

7-4 General Description

The Disk Drive Controller PWA (P/N 1431572), shown in Figure 7-3, supports the two internal 3.5-inch drives. All necessary drivers and receivers are included on the board, allowing direct connection to the drives. The board uses half the standard slot space, and plugs into the primary part of the AT I/O bus. The ACE 25 uses MS-DOS software, under the pSOS operating system, to handle disk drive interfacing. This board uses surface mount technology and cannot be repaired without special equipment. Several versions of this PWA exist; therefore, some boards may vary from the description below.

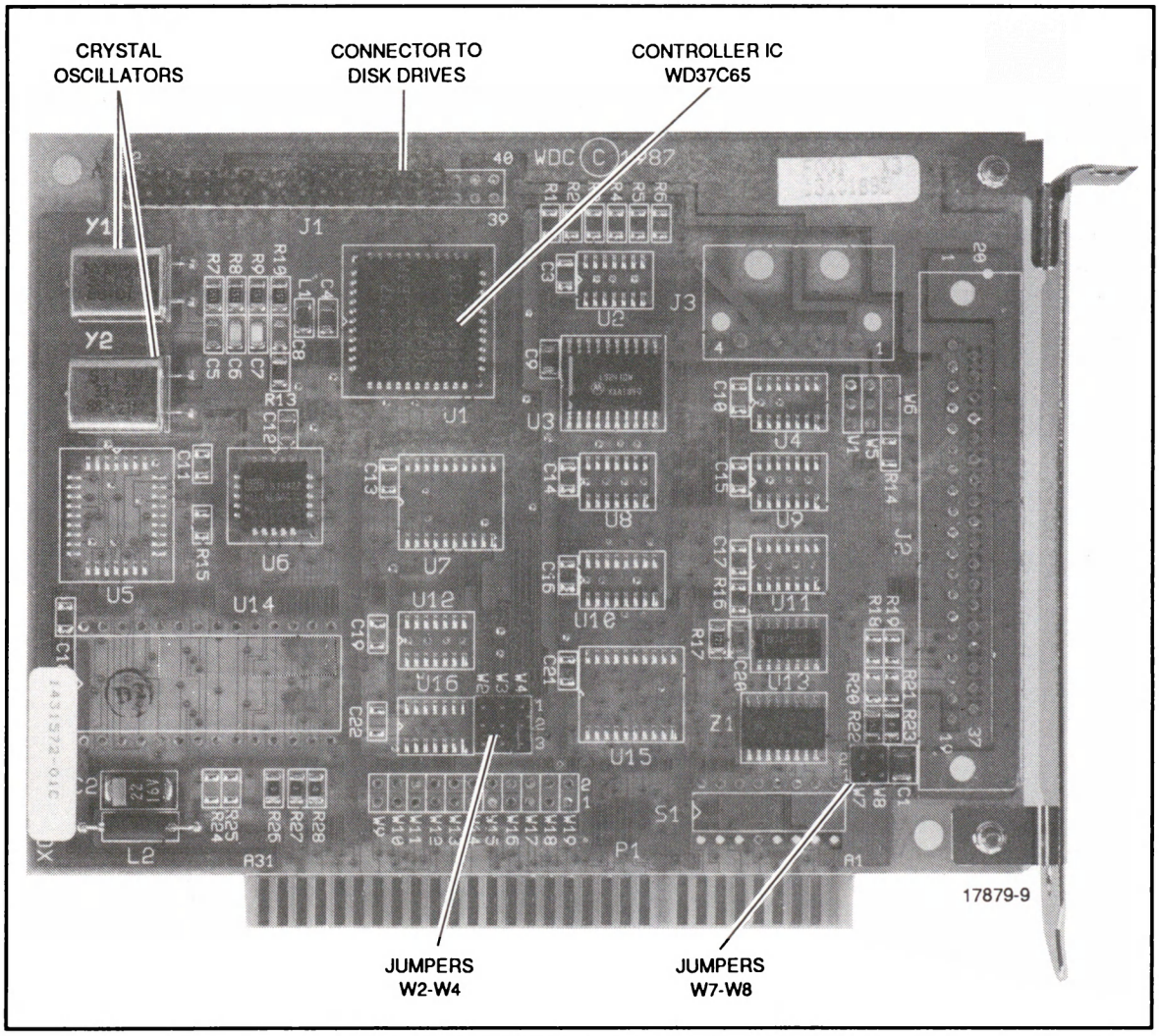


Figure 7-3. Disk Drive Controller PWA

7-5 Theory of Operation

Figure 7-4 is a block diagram of the Disk Drive Controller functions. The BIOS ROM is not used, and there is no external drive connector (J2) and no drive power connector on drives in ACE 25 systems.

Commands, data, and status are communicated to and from the host through I/O port 3F0-3F7 primary (or 370-377 secondary). Address decoding is performed by a PAL (programmable array logic IC) which provides valid address input to the WD37C65A chip, and allows the drive configuration switch S1 to be read by the main CPU. Table 7-3 lists the ports with their register functions. The PAL also combines host bus signals to select the WD37C65A, assert READ or WRITE pins, and load Operation and Control registers.

Table 7-3. Disk Drive Controller PWA Software Ports

Primary	Secondary	Read/Write	Register
3F1	371	Read Only	S1 Drive Configuration Switches
3F2	372	Write Only	Digital Output
3F4	374	Read/Write	Main Status (37C65A)
3F5	375	Read/Write	Diskette Data (37C65A)
3F7	377	Read/Write	Digital Input Diskette Data Rate (37C65A)

The WD37C65A contains all status, control, and data registers. The Main Status register and the Master Status register is read by the CPU before each byte is read from or written into the data register during Command or Result phases. During Execution phase, the Main Status register is not read. The Master Status Register is an eight-bit register with the disk controller status that can be accessed at any time by the CPU. Other status registers (0, 1, 2, 3) are used for error status, track status and head status. The Control register is used to determine the clock rate of data transfer. The Data register stores data, commands , parameters, and FDD status information. The Operations register controls disk drive motor and mode selection.

There are 15 different commands, which have three phases each: Command phase, Execution phase, and Result phase. Each command is initiated by a multi-byte transfer from the processor. The results after execution of the command may also be a multi-byte transfer back to the processor.

The pin connections for the Internal Drive Connector J1 are described in Table 7-4.

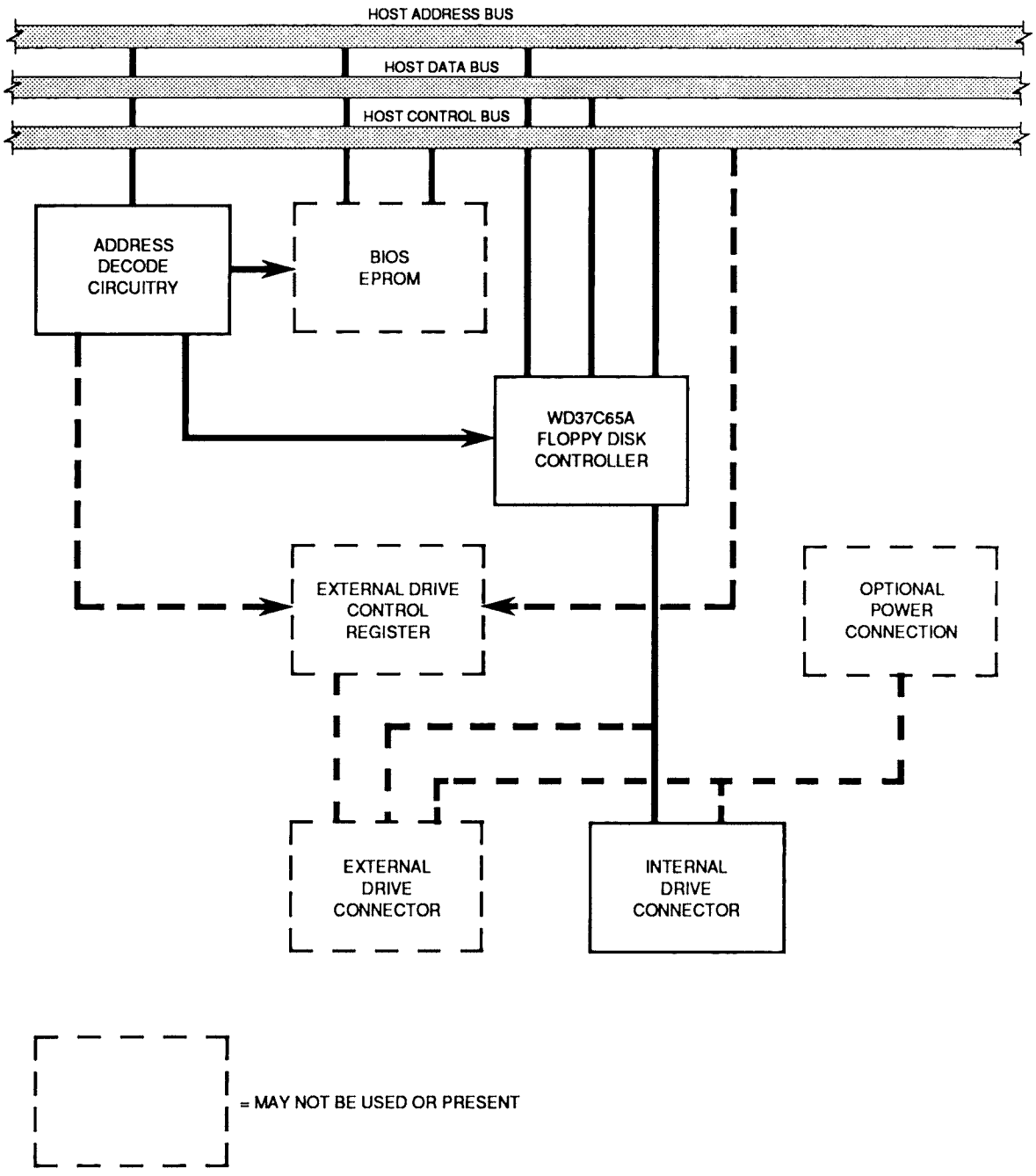


Figure 7-4. Disk Drive Controller Functions Block Diagram

Table 7-4. Disk Drive Controller PWA Pin Connections

Pin No.	Mnemonic	Signal Type	Description of Signal
2	RWC-	Output	Reduced Write Current (Hi-Density)
8	IDX1-	Input	Selected Drive Index
10	M01-	Output	Motor on to First Drive
12	DS2-	Output	Drive Select to Second Drive
14	DS1-	Output	Drive Select to First Drive
16	M02-	Output	Motor on to Second Drive
18	DIRC-	Output	Direction (Low = Move in with Step)
20	STEP-	Output	Step (Move Heads According to DIRC-)
22	WD-	Output	Write Data (Data to be Written)
24	WE-	Output	Write Enable (Allow Drive to Write)
26	TR00-	Input	Track Zero (Heads over Track Zero)
28	WP1-	Input	Write Protect (Disk is Protected)
30	RDD1-	Input	Read Data (Raw Read Data from Drive)
32	HS-	Output	Head Select
34	DISKCHG1	Input	Disk Change (Drive Door was Opened)
38	5VA	Power	+5 Vdc Output to Drive (Optional)
40	+12V	Power	+12 Vdc Output to Drive (Optional)

Note: All Odd-Numbered Pins and Pin 36 are Ground.

7-6 Jumpers

The jumpers are set at the factory and should not be changed.

7-7 MONOCHROME VIDEO DISPLAY ADAPTER PWA

The Monochrome Video Display Adapter PWA (P/N 1431569), shown in Figure 7-5, is a short card located in the I/O Bus of the CPU Motherboard PWA. It contains circuitry used to produce the video display for the data terminal (two terminal displays are supported). Figure 7-6 shows a block diagram of the Monochrome Video Display Adapter PWA.

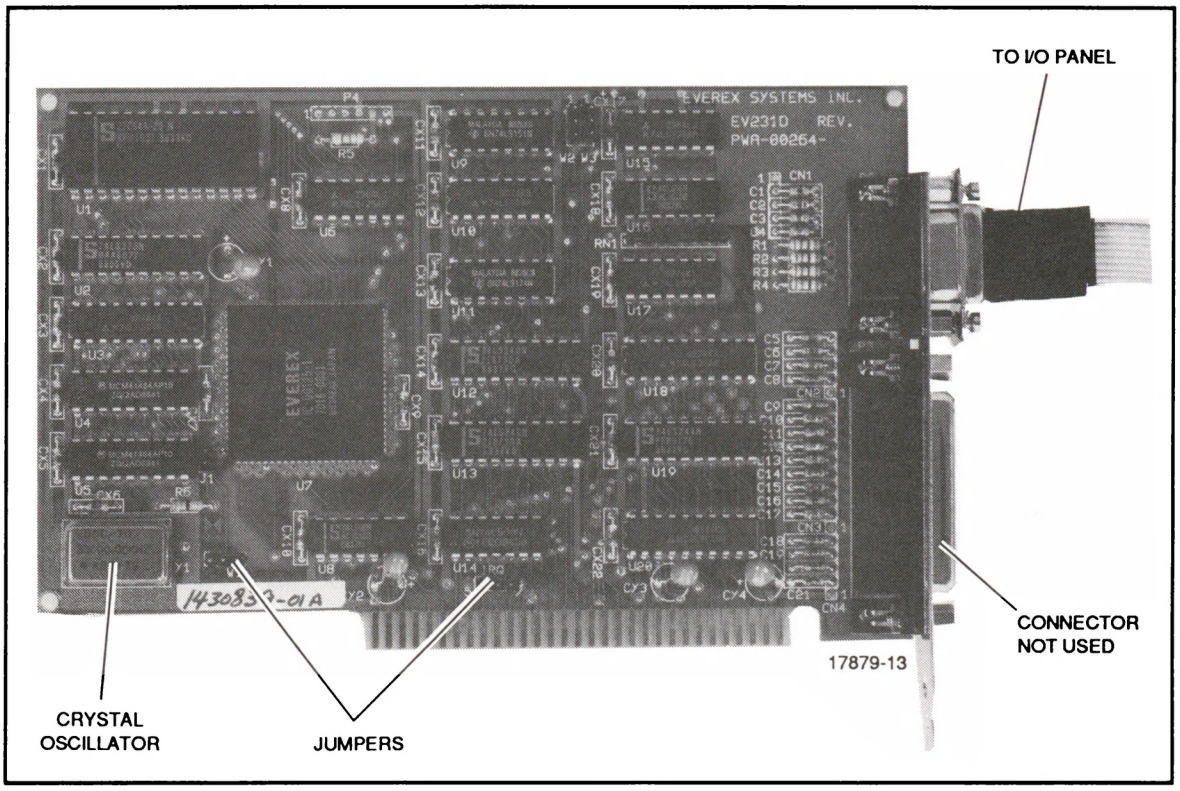


Figure 7-5. Monochrome Video Display Adapter PWA

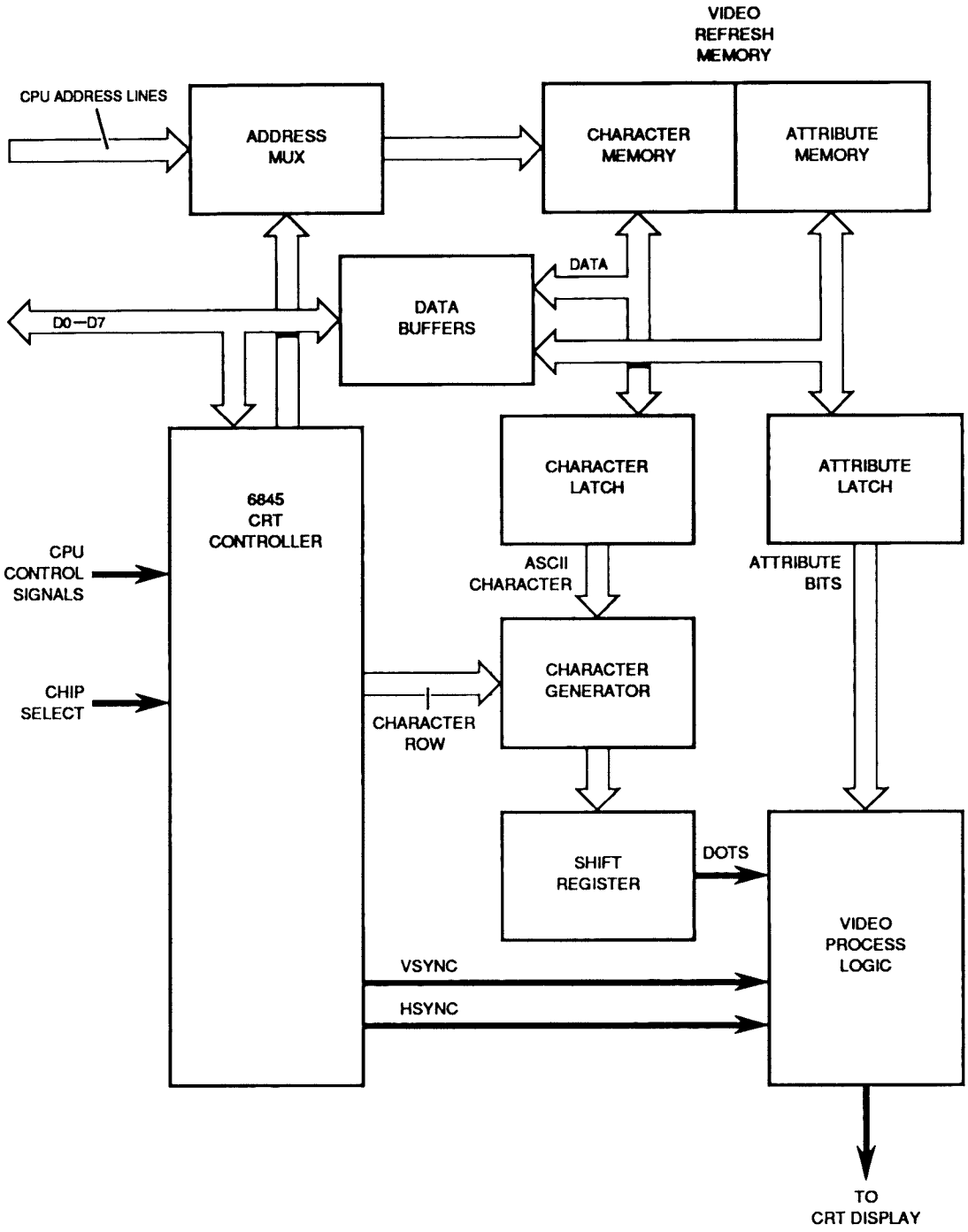


Figure 7-6. Monochrome Video Display Adapter PWA Block Diagram

7-8 Theory of Operation

The 6845 CRT Controller chip provides all the timing and control signals for the video display. The screen refresh RAM on this PWA is dual-ported; it can be accessed by either the CPU or the 6845 CRT Controller. The Address MUX circuitry determines access to the RAM. The contents of the RAM are translated into dot-matrix format by the character generator and shifted out serially in a dot stream to match video timing signals. At the same time a character is read out of memory, its attribute bits (normal, inverted, etc.) are also read out and latched. These bits modify the dot stream (in the video process logic) to produce the final dot stream sent to the CRT for display.

7-9 Jumpers

Set the jumpers listed below as follows:

J1 — ON Position

W1 — BC Position

W2 — BC Position

W3 — BC Position

IRQ — 6-7 Position

SECTION 8

COLOR FIELD 1 DETECTOR PWA

8-1 INTRODUCTION

The major function of the Color Field 1 Detector PWA (P/N 1431454), shown in Figure 8-1, is to detect field 1 timing from the reference video input signal. This timing information is used to synchronize internal field signals. The Color Field 1 Detector PWA is also called the Color Framer PWA, or the Color Field 1 ID Detector PWA.

Other functions of the Color Field 1 Detector PWA include the General Purpose Interface (GPI) ports, with related latches and drivers, and the battery-backed RAM (random access memory) used to retain system data.

8-2 THEORY OF OPERATION

Figure 8-2 is a block diagram of the major board functions. The major circuits are: Sync and Burst Separator; Sync Processor and Line Selector; Burst Processor; Burst Edge Sampler, Burst Phase Comparator; T-Pulse Generator; State Machine; Line Counter; Field Counter Status Latch; GPI; I/O Enables; and Battery-Backed RAM.

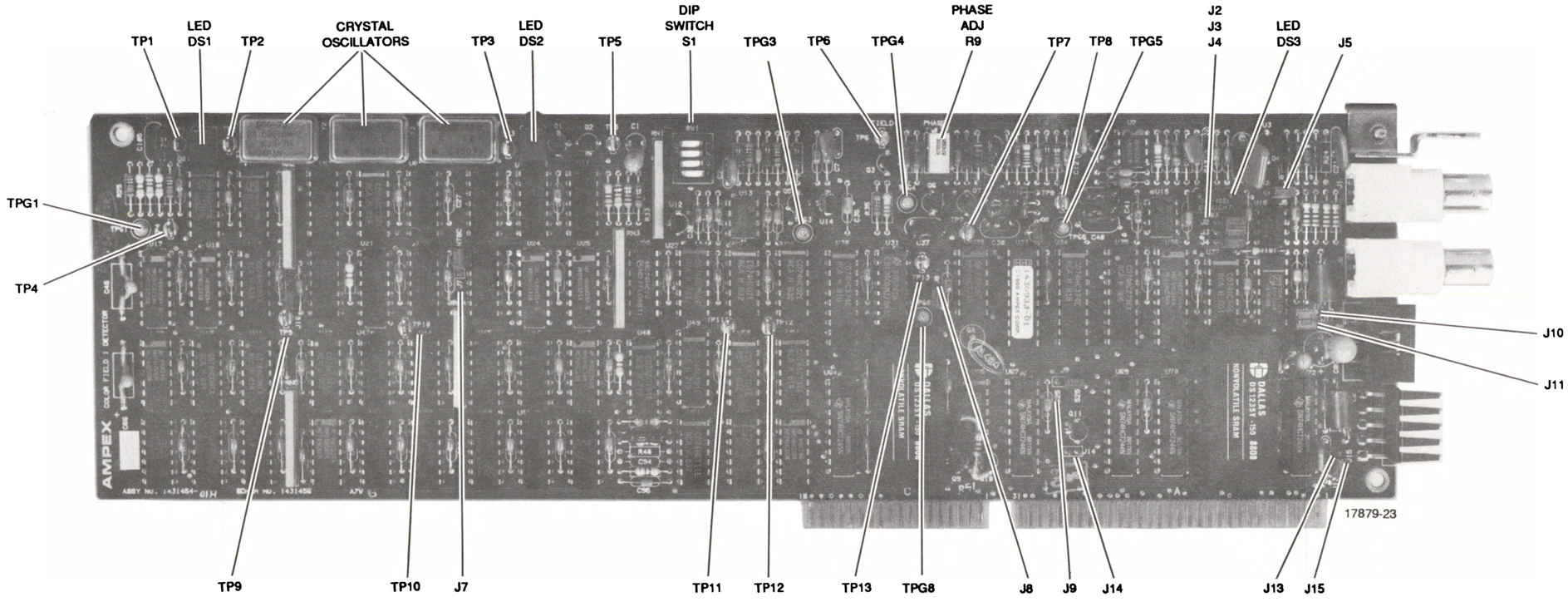


Figure 8-1.
Color Field 1 Detector PWA

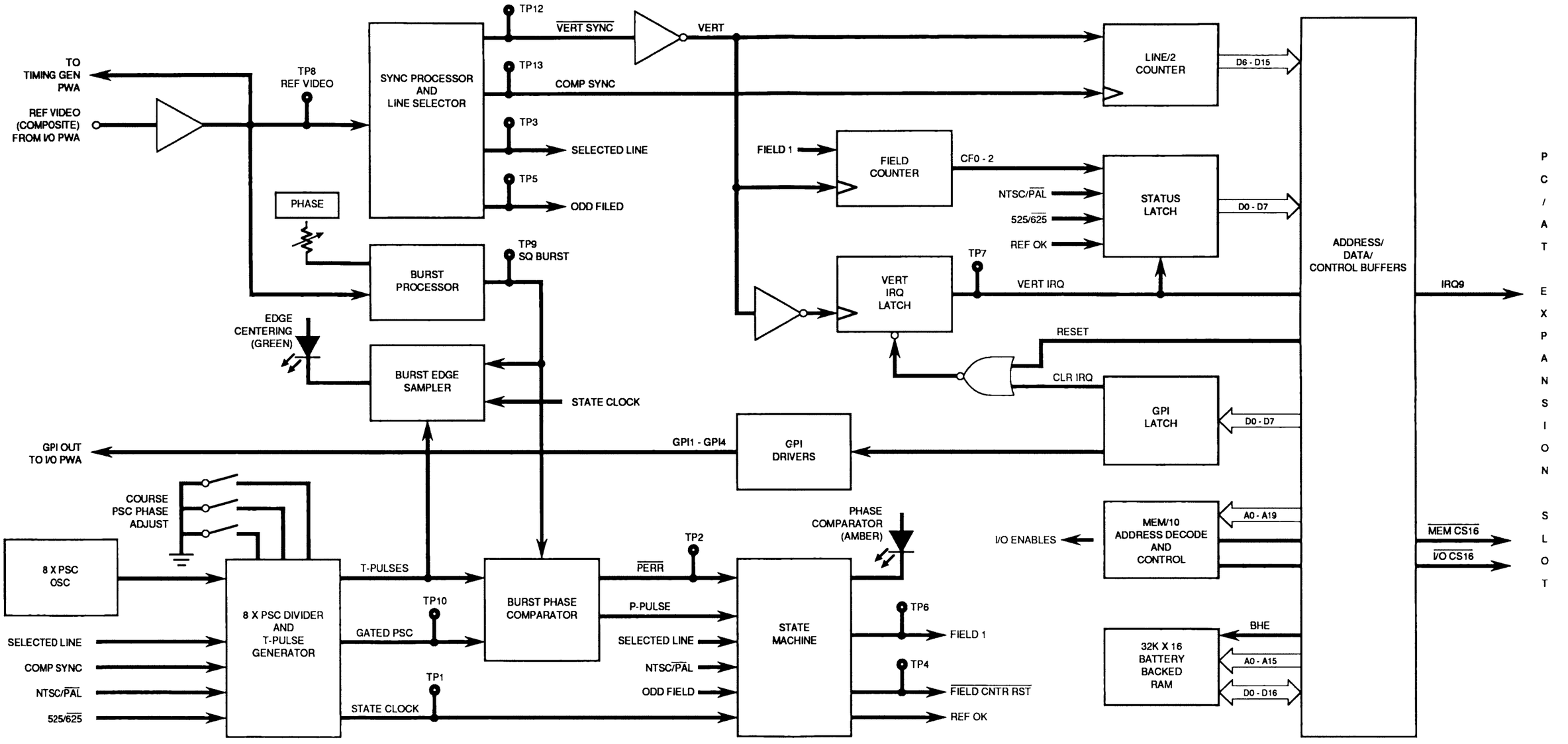


Figure 8-2.
Color Field 1 Detector PWA
Block Diagram

8-3 Color Field 1 Detection

Reference video (one volt peak-to-peak terminated) enters through connector J6, and can be either EIA Standard RS-170A for NTSC, or EBU PAL signal, or comparable, for PAL-M signal. In many component video applications, the input reference video signal is a composite black burst signal. A component black signal with no burst can be used, in which case the burst processing circuitry is bypassed. When the burst processing circuitry is bypassed, no valid color frame identification exists and the video signal output is locked up to sync timing only, instead of locking to the entire set of timing signals.

The reference video enters the Sync and Burst Separator at emitter-follower Q4, which buffers the video. The reference video signal is passed on to the Timing Generator PWA through connector J1.

The sync separator chip (U2) processes this signal to extract four signals. Negative vertical sync (VERT SYNC) can be checked at TP12. Composite sync (COMP SYNC) appears at TP13. The odd field signal is on TP5, and is high when odd field is true (field 1-3-5-7 for PAL). TP3 shows the selected line (line 22 for NTSC or line 21 for PAL) used by the line counter. Jumper J16 in the alternate position creates a continuous selected line signal for test purposes. The odd field signal is also used in the state machine.

Burst gate is fed to Q5 to turn a comparator (U13) on or off during burst interval. TP11 displays burst gate. More circuitry in the burst processor (C9, R11, and Q6) drives the phase shifting potentiometer (R9), which is used for fine adjustment of phase. The square burst signal, without chroma information, can be checked at TP9.

The Burst Edge Sampler circuit (including U9, U20, Q1, and Q2) uses the square burst signal as an input, plus two different phases of T-pulses (from the T-Pulse Generator), to make a comparison. A green LED on the edge of the PWA remains lit while the square burst signal is centered in the window produced by the two T-pulses, to aid in burst phase adjustment. (R9 and S1 are used to adjust for maximum light duration.)

The T-Pulse Generator circuit receives an 8X subcarrier frequency from a set of three crystal oscillators (NTSC, PAL, PAL-M), selected via U7/U21, which decodes jumpers J9 (525/625) and J7 (NTSC/PAL). The output of U10 is the primary 8X subcarrier clock which provides a stable count down from the leading edge of horizontal sync. U46, U48, and U49 are used to produce proper timing signals. Switch S1 adjusts the delay in 1/8-subcarrier cycle increments (only three positions are used). A series of T-pulses are generated to sample timing (U43, U48, U45, and U22), going to the Burst Edge Sampler, the Burst Phase Comparator, and the state machine. TP10 is the gated subcarrier, while TP1 is the state clock signal.

The Burst Phase Comparator uses the square burst signal, T-pulses, and the gated subcarrier signal (Fsc). This circuit takes the incoming square burst and compares that with the Fsc (gated subcarrier) of TP10. An output signal (P-Pulse and its complement P-NOT), is produced and fed to the state machine (check at TP2). In NTSC, P is low at the start of field 1, and high for field 3, and P-NOT is the opposite. For PAL, the pattern is different. Another signal indicating pulse error is developed, which goes low whenever the input burst is missing or its phase has shifted too much. The phase error signal is used to reset the state machine and trigger the yellow phase comparator warning lamp.

Figure 8-3 shows the state machine diagram and logic table for PAL . The state machine inputs are the T-pulses and error signal from the burst phase area, the selected line signal, the NTSC/PAL signal, and the odd field signal. The state machine runs until it produces a field 1 reset pulse, or is reset externally. Field 1 is identified as an output from field counter flywheel U18. Losing sync momentarily will not necessarily disrupt the field count flywheel output. The field 1 signal on TP6 is present each time the flywheel counter reaches that point in the count cycle.

The field counter reset signal (FIELD CNTR RST) is created by the state machine, and can be checked at TP4. The field 1 reset pulse continually re-triggers the Reference OK one-shot. If the one-shot times out, the Reference OK signal goes low (false) and is detected by the CPU, which notifies software that reference is not reliable.

The Line Counter circuit counts TV or H lines (U31) divided by 2, and is fed through a latch (U30) linked to the PC bus, to be read by software. This circuit is clocked by comp sync and reset by the vertical sync. The first few line counts will be irregular, then the count stabilizes.

The Field Counter Status latch (U66) uses vertical sync to clock fields, and is reset by the field 1 and line 8 signals. The output signal (CF01/CF02) is fed to a status latch which can be read by software through the PC bus.

The vertical latch (U32) is set at the beginning of vertical sync, causing the vertical interrupt signal to go true. The vertical interrupt signal (TP7) is passes through jumper J8 (where it can be disabled for troubleshooting) onto pin B4 of the PC bus, causing an interrupt in software (vertical interrupt). The software disables this interrupt by writing a 1 to data bit 0 in latch U35 (the GPI latch), which clears the interrupt (CLR IRT).

LOGIC TABLE

LAST STATE			INPUT	FLIP-FLOP INPUTS						NEXT STATE		
$Ø_A$	$Ø_B$	$Ø_C$	P_A	J_A	K_A	J_B	K_B	J_C	K_C	$Ø_A$	$Ø_B$	$Ø_C$
0	0	0	0	0	1	0	0	0	1	0	0	0
0	0	0	1	0	1	0	0	1	1	0	0	1
0	0	1	0	0	1	0	1	0	1	0	0	0
0	0	1	1	0	1	1	1	1	1	0	1	0
0	1	0	0	0	1	0	0	1	1	0	1	1
0	1	0	1	0	1	0	0	0	0	0	1	0
0	1	1	0	1	1	0	1	1	1	1	0	0
0	1	1	1	0	1	1	1	0	0	0	0	1
1	0	0	0	0	1	0	0	0	1	0	0	0
1	0	0	1	0	1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1	0	1	0	0	0
1	0	1	1	0	1	1	1	1	1	0	1	0
1	1	0	0	0	1	0	0	1	1	0	1	1
1	1	0	1	0	1	0	0	0	0	0	1	0
1	1	1	0	1	1	1	1	1	1	0	0	0
1	1	1	1	0	1	1	1	0	0	0	0	1

$J_A = Ø_C \bullet Ø_B \bullet -P$
$K_A = 1$

$J_B = P \bullet Ø_C$
$K_B = Ø_C$

$J_C = P \bullet -Ø_B + -P \bullet Ø_B$
$K_C = -P \bullet -Ø_B$

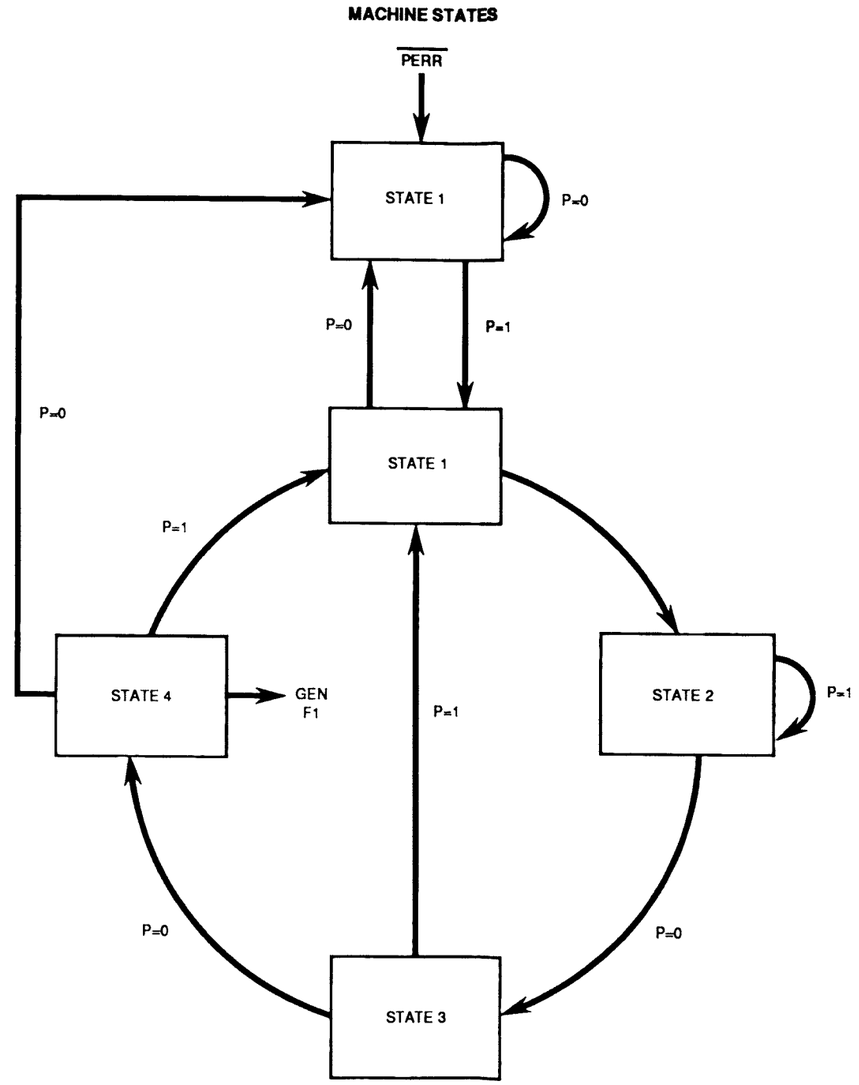


Figure 8-3.
State Machine Logic Table and Diagram (PAL)

8-4 GPIs

The GPIs are independent of the other functions on this board. Data from the gated bus passes through the bus transceivers (U72 and U64), and is written to a latch (U35) at data bits 4 through 7; Address decoder U33 determines the correct GPI, plus a color frame decode. Status latch U34 holds field, television standard, reference ready, and other data. The outputs are fed through inverter U37 and jumpers J2, J3, J4, and J5, to the actual bus drivers (U15 and U16). The data is sent to the Input/Output PWA via connector J12. An LED (D3) has one section for each GPI trigger, which lights when the trigger is on.

8-5 Battery-Backed RAM

The remaining function on this board is the battery-backed RAM, made up of two 8-bit x 32 Kbyte combination RAM/battery pack chips. U70 stores the high bytes for data bits 8 through 15, while U71 stores the low bits 0 through 7. The two chips are accessed together and decoded by U62, for either 8-bit or 16-bit data transfers. Signal CS16 on pin D1 is pulled low when there is a 16-bit data transfer to the PC bus.

8-6 COLOR FIELD 1 DETECTOR PWA ADJUSTMENTS

The Color Field 1 Detector PWA may have to be adjusted to operate correctly with the reference video signal used at the location where the system is installed. The following paragraphs describe these adjustments.

8-7 Video Reference

The adjustment procedure is the same for NTSC, PAL, and PAL-M. A 1-volt black burst or bars video signal is required. For reference, an independent field 1 reference signal from a sync generator or VTR is needed.

Note

Be sure input video is terminated properly before starting adjustments, as changes in signal amplitude will cause changes in SC/H phase relationship.

8-8 Standards Jumpers

The TV line standards jumpers J7 and J9 must be set to the proper configuration. J7 is set to position BC for NTSC, and position AB for PAL. J9 is set to position AB for 625, and position BC for 525.

Make sure the Vertical Interrupt jumper J8 is in the AB position.

8-9 Hysteresis Adjustment

Early "B" version artwork has a 200-ohm pot (R6) which was used to slightly alter the hysteresis in the burst squaring comparator (U13). If this pot has not been removed, it should be set so that the negative-going burst gate pulse applied to U13 pin 5 goes down to +0.5 V or lower during the burst interval.

8-10 SC/H Phase Adjustment

To pick a nominal "center point" to start, set DIP switch SW1 sections 1 and 2 to ON, and section 3 to OFF; section 4 is not connected. Switch SW1 selects 1 of 8 delay increments to put the phase adjust pot R9 near the center of its range. Set this 20-turn pot near mid-range and observe the burst R4 (located on top edge of PWA). Burst amplitude will be between 350 and 500 millivolts.

Adjust SW1 to bring the Field 1 pulse at TP6 into agreement with the reference Field 1 signal. The green Edging Centering LED and the amber Phase Error LED may be on, off, or blinking. Adjust SW1 to minimize the amber LED on duration, while maintaining the proper field 1 relationship with the field 1 reference signal. Final adjustment is made using phase adjust pot R9, to achieve the maximum green LED on duration. If the end of pot range is reached, the next setting on SW1 is used to allow re-centering of R9. Repeat process as needed.

8-11 TEST POINTS

Table 8-1 lists the test points located on the Color Frame 1 Detector PWA.

Table 8-1. Color Field 1 Detector PWA Test Points

Test Point	Signal Name
TP1	State Clock
TP2	Phase Error
TP3	Selected Line Signal
TP4	Negative Field Counter Reset
TP5	Odd Field
TP6	Field 1
TP7	Vertical Interrupt True
TP8	Reference Video Input
TP9	Square Burst
TP10	Gate Sub-Carrier Frequency
TP11	Burst Gate
TP12	Negative Vertical Sync
TP13	Composite Sync

8-12 GPI INTERFACING

The bottom DB-25 connector on the rear panel of the ACE 25 edit controller is the General Purpose Interface (GPI) port. This GPI port is used to control external devices through four outputs, plus +5 volts power and ground. Figure 8-4 shows the signals on the connector pins. The GPI ports can be jumpered on the Color Field 1 Detector PWA to be either positive- or negative-triggered. A typical application is illustrated in Figure 8-5.

NAME	POSITION
GPI-1	1
GPI-2	2
GPI-3	3
GPI-4	4
+5V (CL)	5
GROUND	14, 15, 16, 17, 18

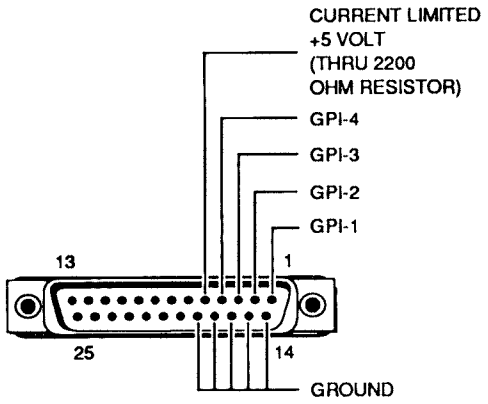


Figure 8-4. GPI Connector Pin Signals

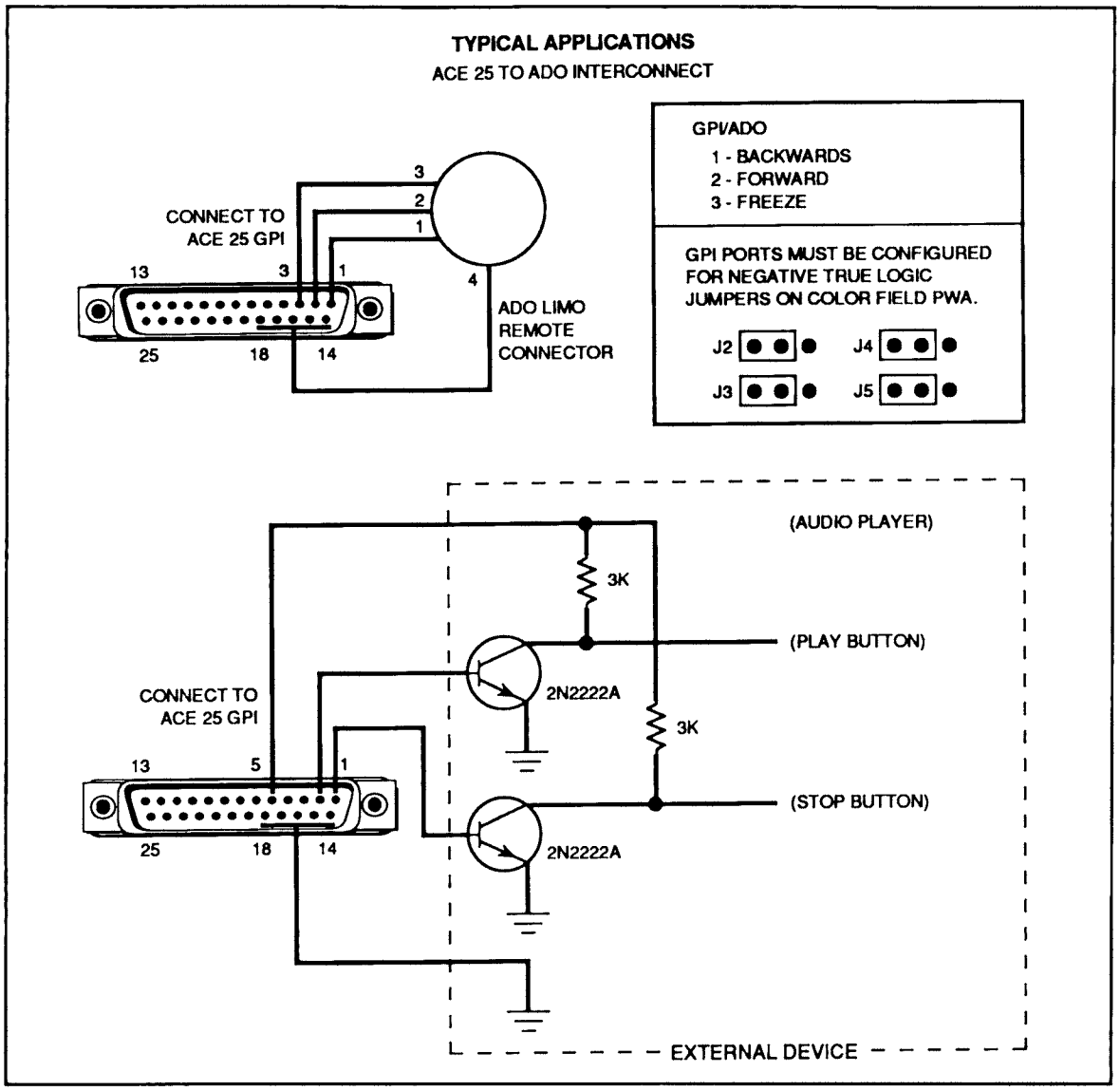


Figure 8-5. Typical GPI Application Interface Diagram

SECTION 9

VIDEO TIMING PWA

9-1 INTRODUCTION

The Video Timing PWA (also called the Video Timer PWA), develops key video timing signals for internal use from the external reference video signal. There are two different versions of this PWA:

- Component Video Timing PWA (P/N 1445955)
- Composite Video Timing PWA (P/N 1443382)

9-2 COMPONENT VIDEO TIMING PWA

The Component Video Timing PWA is used in component systems only. The following paragraphs describe the circuitry of this PWA and provide adjustment procedures to set correct video timing. Figure 9-1 shows the Component Video Timing PWA and identifies key components.

9-3 General Description

The Component Video Timing PWA produces seven outputs: Black, U-Sub, V-sub, composite blanking pulse (CBP), short composite blanking pulse (SCBP), clamp pulse (CLMP), and clamp sync pulse (CSP). The U-Sub and V-Sub signals are not used on this PWA. Typically, a composite reference video signal is used as the input. Figure 9-1 shows this PWA and identifies key components.

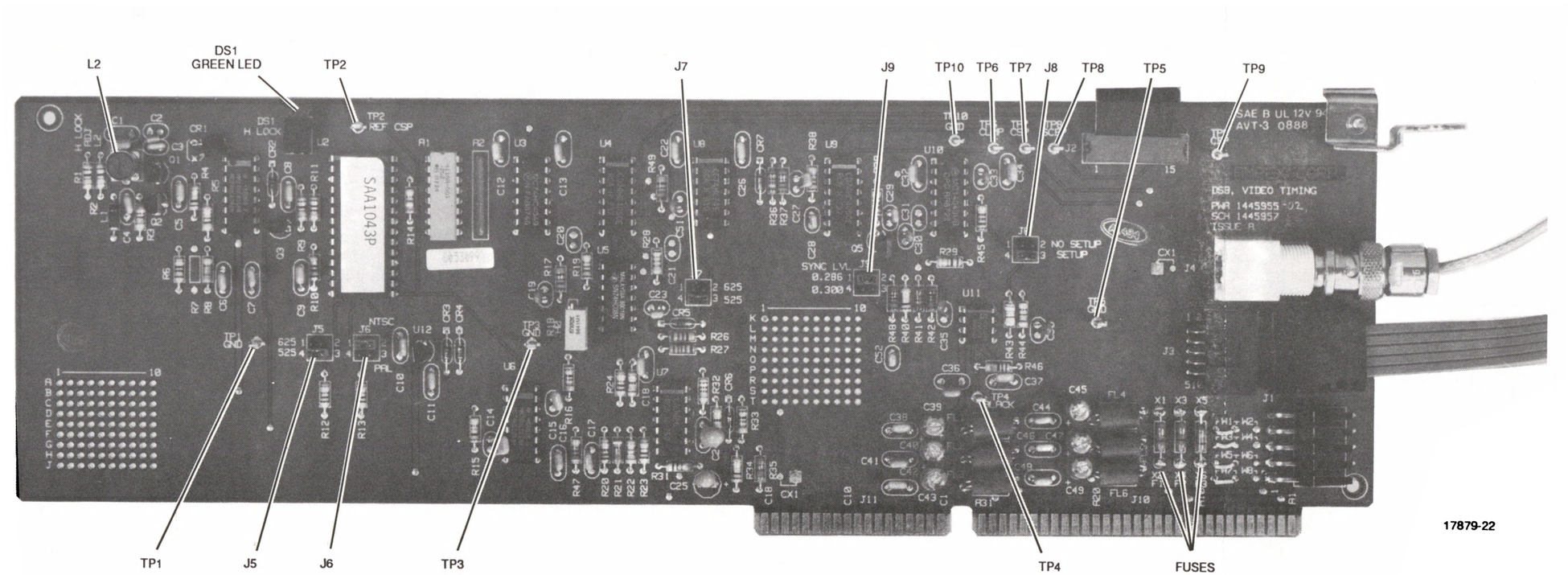


Figure 9-1.
Component Video Timing PWA

9-4 Theory of Operation

Figure 9-2 presents a simplified block diagram of the Component Video Timing PWA. The main circuits on the PWA comprise:

- Input Sync Stripper
- Half-Line Delete and Horizontal Phase Adjustment
- Horizontal Phase Comparator
- Sync Generator
- Sync Width Correction
- Composite Blanking/Short Composite Blanking circuits

Three fuses (F1, F2, and F3) are used to protect against power overloads.

9-5 Input Sync Stripper Circuit

Reference video enters this board through connector J4 from the Color Frame 1 Detector PWA, as a terminated one volt peak-to-peak signal. The video signal comes through C25 and is ac-coupled, then the dc operating point is set in U7. The signal is inverted and buffered, and sync tip set slightly above zero volts, producing a composite sync signal ranging from 0 to 5 volts. This signal goes into two circuits: the Half-Line Delete and the Sync Generator circuits. TP2 displays the reference clamp sync pulse signal (REF CSP).

9-6 Half-Line Delete and Horizontal Phase Adjustment

The REF CSP signal enters this circuit on pin 10 of U6. The half-lines and vertical interval are deleted into the first part of U6. The output then goes to pin 2 of U6, with an adjustment at R18 of approximately ±1 µs in the H-phase. This adjustment allows the internal switcher block to match up horizontally with other switcher inputs. The horizontal reference output from U6 is roughly 1 whole line delay from the REF CSP test point, and is the output that goes into the Horizontal Phase Comparator circuit.

9-7 Horizontal Phase Comparator

A phase-lock loop is created between the Horizontal Phase Comparator and the Sync Generator circuits. The horizontal reference signal comes in on pin 14 of U1 (Phase Comparator). For a comparison signal, the clamp signal from U2 (Sync Generator) is brought into pin 3 of U1. The phase comparison output goes into a filter network (R5, R8, C6) to develop a dc error voltage, which goes into an oscillator circuit via R4. This oscillator is tuned with L2 to produce the best phase-lock condition, by lighting the H-lock LED (DS1), and setting the adjustment to mid-position. The output of the oscillator circuit is fed to U2 to provide the clock rate and signal output timings, to complete the phase-lock loop.

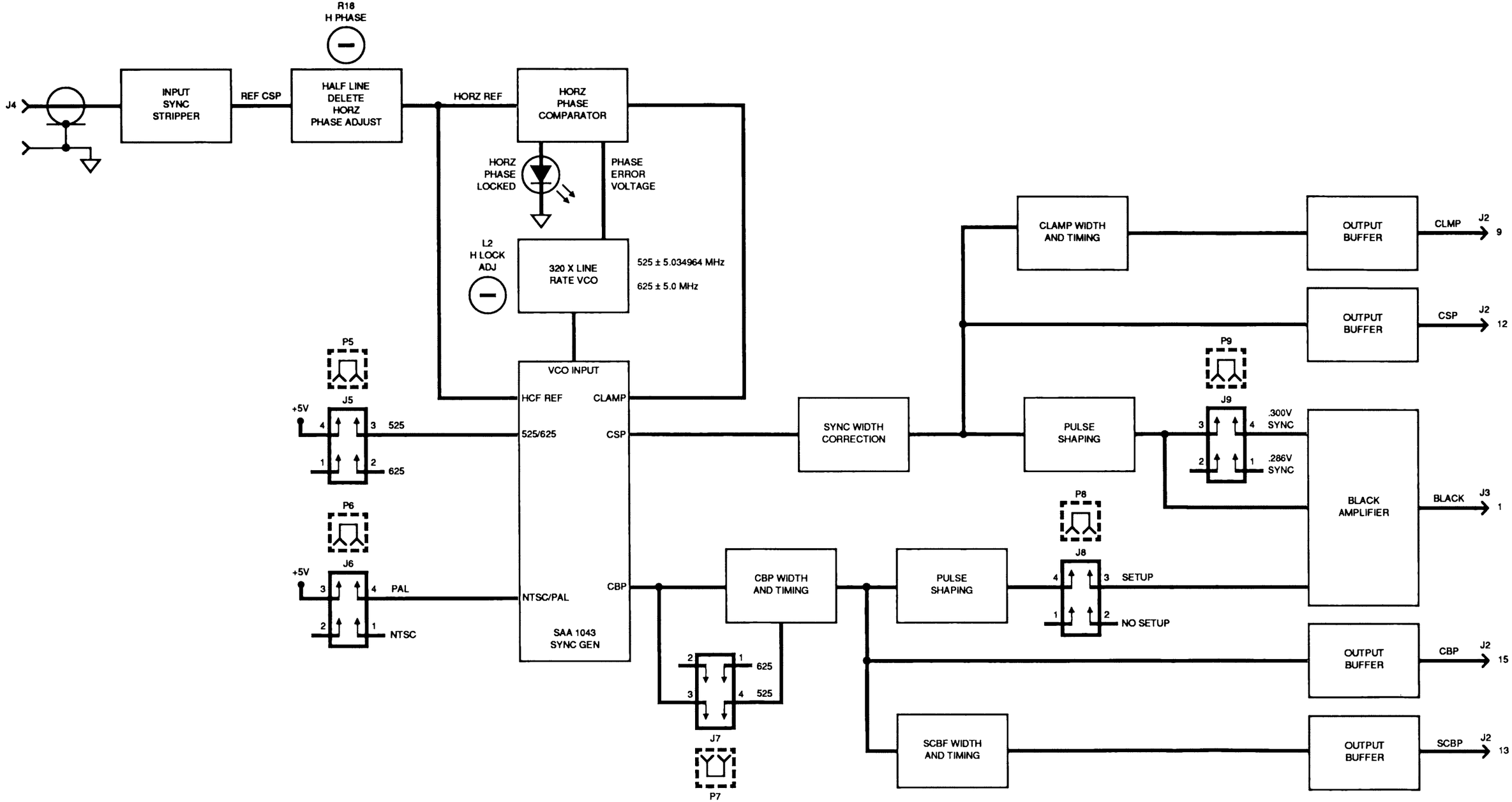


Figure 9-2.
Component Video Timing
PWA Block Diagram

9-8 Sync Generator

This circuit generates the clamp, clamp sync pulse (CSP), and composite blanking pulse (CBP) signals. The REF CSP signal from the Half-Line Delete circuit comes into U2 at pin 15. Jumpers J5 (525/625) and J6 (NTSC/PAL) are used to set the television standard for U2. Input Vcc voltage of 6.4 volts comes from U12, and all outputs of U2 are also 6.4 volts, which is divided down to 0.5 volts by resistor/divider networks A1 and A2. As mentioned earlier, the clamp signal is sent over to the Phase Comparator circuit to make a phase-lock loop.

The CSP output is routed to the Sync Width Correction circuit. The CBP signal is sent to the Composite Blanking circuit.

9-9 Sync Width Correction

The CSP signal from U2 goes through a buffer (U4), into a circuit which corrects the width (CR7, R36, R37). U9 then re-shapes the signal, which is sent to two locations. One path goes through a delay circuit (R38, C28) into a buffer and finally is routed to the video switcher via pin 11 of connector J2. The second path is to U10 and R45, where the signal is inverted and edges sharpened. The signal then goes into the Black op-amp, and then into buffer U11A, where it joins the signal from the Composite Blanking circuit.

Going back to U9, the CSP signal also branches to C31 and Q5, to develop a clamp pulse at end of sync. Two resistor-capacitor networks (R40/C31 and R39/C29) set the width and timing. The clamp pulse is buffered, then goes to the video switcher via pin 9 of connector J2.

9-10 Composite Blanking Pulse/Short Composite Blanking Pulse

The composite blanking pulse (CBP) from U2 goes to U4. Jumper J7 (525/625) together with R27 and R26, sets the horizontal blanking width of the CBP. The signal re-enters U4 for shaping, is delayed through U49/C51, then goes back into U4 for re-shaping, to emerge as the output composite blanking pulse (CBP). The R28/C21 delay is not needed to match this CBP with the CSP signal. The final CBP signal can be checked at TP9, before going to the video switcher via pin 15 of connector J2.

The CBP signal is also routed from U4 to network R29/C33 for shaping. Jumper J8 is sued to select setup or no setup. If the jumper is in the setup position, the shaped CBP travels through R43 into the op-amp, and has a black setup of 7.5 IRE.

The shortened composite blanking pulse (SCBP) is developed from the CBP. A delayed CBP is fed into pin 1 of U5, while an earlier CBP enters on pin 2. The shortened composite blanking pulse goes from pin 3 of U5, through a delay (R19/C20), into a buffer. The SCBP can be checked at TP8 before going to the video switcher via pin 13 of connector J2.

9-11 Component Video Timing PWA Test Points, Jumpers and Adjustments

Table 9-1 lists the test points of the Component Video Timing PWA, Table 9-2 lists the jumpers, and Table 9-3 lists the adjustment points.

Table 9-1. Component Video Timing PWA Test Points

Test Point	Signal Name
TP1	GND (Analog Ground)
TP2	REF CSP (Reference Composite Sync Pulse)
TP3	GND (Analog Ground)
TP4	BLACK
TP5	GND (Analog Ground)
TP6	CLMP (Clamp Pulse)
TP7	CSP (Composite Sync Pulse)
TP8	SCBP (Short Composite Blanking Pulse)
TP9	CBP (Composite Blanking Pulse)
TP10	GND (Analog Ground)

Table 9-2. Component Video Timing PWA Jumpers

Jumper	Description
J5	Selects 625/525 Line Rate: Position 1-2 (625) Position 4-3 (525)
J6	Selects NTSC/PAL: Position 1-2 (NTSC) Position 4-3 (PAL)
J7	Selects 625/525 Line Rate: Position 1-2 (625) Position 4-3 (525)
J8	Selects Setup/No Setup: Position 1-2 (No Setup) Position 4-3 (Setup)
J9	Selects Sync Level: Position 1-2 (0.286V) Position 4-3 (0.300V)

The Horizontal Lock Adjustment is made using the following procedure:

1. Turn L2 on the Component Video Timing Generator PWA in each direction to determine the range in which the green H LOCK LED (DS1) is lit.
2. Set L2 to the mid-range position. H LOCK LED should remain lit.

The Horizontal Phase Adjustment is made using the following procedure:

1. Connect TP4 (Black) on the Component Timing Generator PWA to one probe of an oscilloscope.
2. Connect the other probe of the oscilloscope to one of the switcher video inputs.
3. Turn R18 on the Component Timing Generator PWA to match the horizontal phase of the two signals on the oscilloscope as closely as possible.
4. Repeat procedure for remaining switcher video inputs.
5. When adjustment is completed, signal at TP4 should have approximately one line delay from input Reference Video signal.

Table 9-3. Component Video Timing PWA Adjustment Points

Point	Description
L2	H LOCK ADJ — Horizontal Lock Adjustment
DS1	H LOCK LED (Green) — Horizontal Lock Indicator
R18	H PHASE ADJ — Horizontal Phase Adjustment
F1	5 amp fuse (+15V)
F2	5 amp fuse (+5V)
F3	5 amp fuse (–15V)

9-12 COMPOSITE VIDEO TIMING PWA

The Composite Video Timing PWA supports either composite or component systems. The following paragraphs describe the circuitry of this PWA, and provide adjustment procedures to set correct video timing. Figure 9-3 shows the Composite Video Timing PWA and identifies key components.

9-13 General Description

The Composite Video Timing PWA produces eight outputs: Black, -U Sub, V Sub, composite blanking pulse (CBP), composite sync pulse delayed (CSPD), short composite blanking pulse (SCBP), clamp pulse (CLMP), and clamp sync pulse (CSP). Typically, a composite reference video signal is used as the input.

9-14 Theory of Operation

Figure 9-4 presents a simplified block diagram of the Composite Video Timing PWA. The main circuits on the PWA comprise:

- Input Sync Stripper
- Half-Line Delete and Horizontal Phase Adjustment
- Horizontal Phase Comparator
- Sync Generator
- Sync Width Correction
- Composite Blanking/Short Composite Blanking circuits
- Burst Gate
- Set ID
- Field 1 Enable
- Chroma Phase Adjustment
- Band Pass Filter

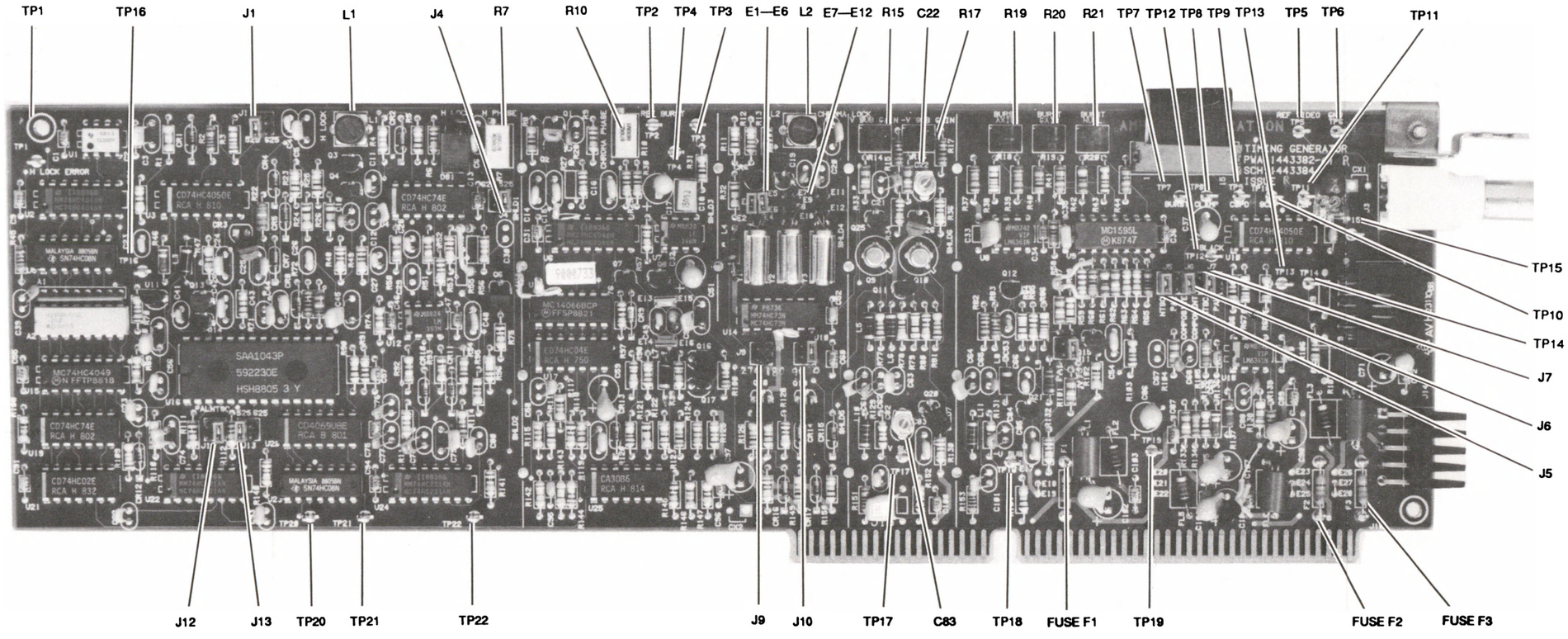


Figure 9-3.
Composite Video Timing PWA

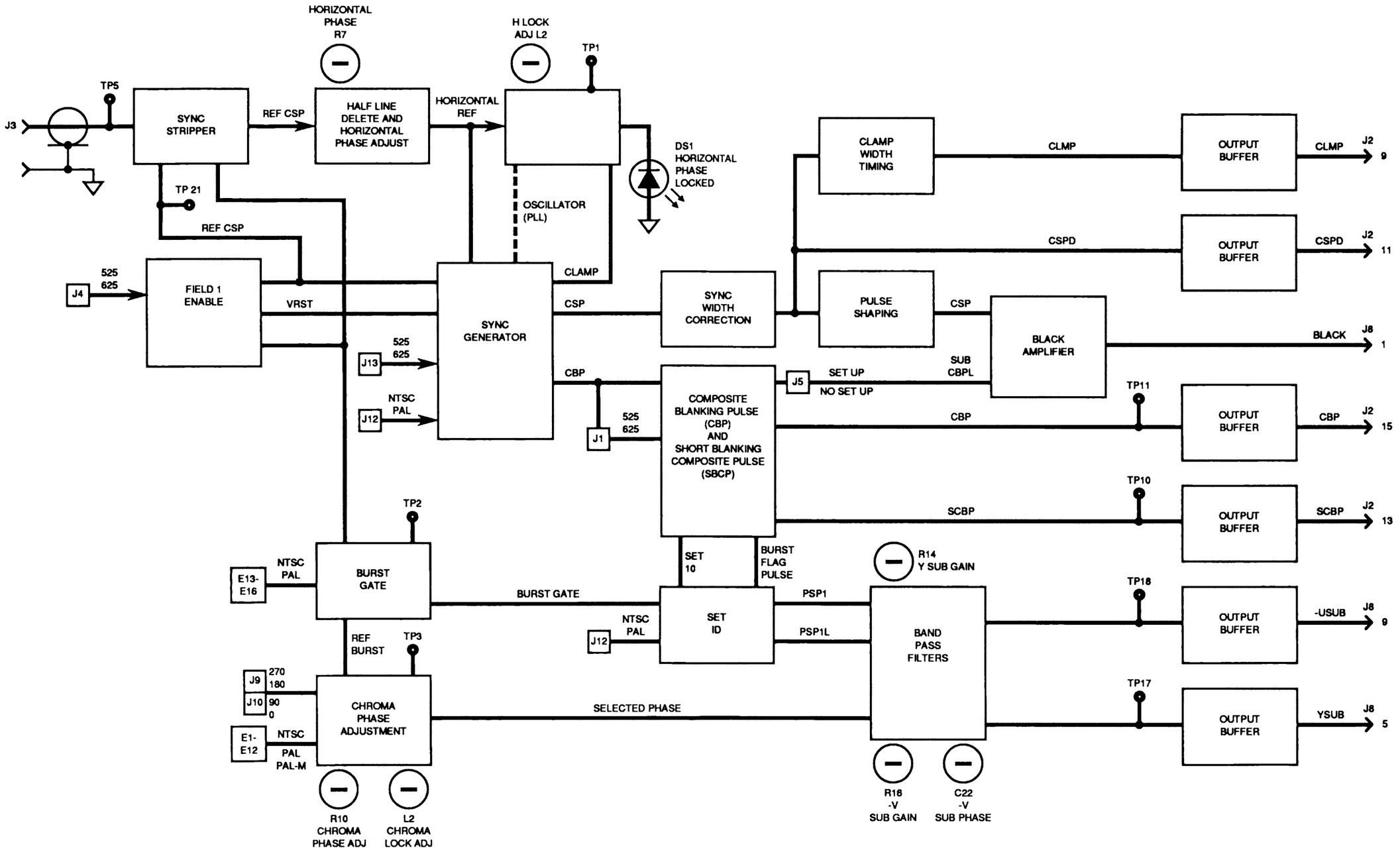


Figure 9-4.
Composite Video Timing PWA
Block Diagram

9-15 Sync Stripper Circuit

Reference video enters through connector J3 as a terminated one volt peak-to-peak signal (TP5). The video signal is ac-coupled, then the dc operating point and gain are set. The signal is next inverted and buffered, and sync tip set slightly above zero volts, producing a composite sync signal ranging from 0 to 5 volts. This signal goes into two circuits: the Half-Line Delete circuit and the Sync Generator circuit. TP21 displays the reference clamp sync pulse signal (REF CSP).

9-16 Half-Line Delete and Horizontal Phase Adjustment Circuit

The half-lines and vertical interval are deleted in the first part of U24. R7 allows a ±1 μs adjustment in the H phase, to allow the internal switcher block to match up horizontally with other switcher inputs. The horizontal reference output from U24 is roughly 1 whole line delay from the REF CSP test point, and is sent to the Horizontal Phase Comparator circuit.

9-17 Horizontal Phase Comparator Circuit

A phase-lock loop is created between the Horizontal Phase Comparator and the Sync Generator circuits. The horizontal reference signal comes in on pin 14 of U2 (Phase Comparator). For a comparison signal, the clamp signal from U16 (Sync Generator) is brought into pin 3. The phase comparison output goes to a filter network to develop a 3 Vdc error voltage (TP1), which goes to an oscillator circuit via R24. This oscillator is tuned with L1 to produce the best phase-lock condition, by lighting the H-Lock LED (DS1) then setting the adjustment to mid-position. The output of the oscillator circuit is fed to U16 to provide the clock rate and signal output timings, to complete the phase-lock loop.

9-18 Sync Generator Circuit

This circuit is based on U16; it generates video timing signals such as clamp, clamp sync pulse (CSP), and composite blanking pulse (CBP). The REF CSP signal from the Half-Line Delete circuit comes in at pin 15. Jumpers J13 (525/625) and J12 (NTSC/PAL) set the television standard. Input voltage Vcc and all outputs are 6.4 volts, which is divided down to 0.5 volts by resister/divider networks A1 and A2. As mentioned earlier, the clamp signal is sent to the Phase Comparator circuit to complete a phase-lock loop. The CSP signal is routed to the Sync Width Correction circuit. The CBP signal is sent to the Composite Blanking circuit.

9-19 Sync Width Correction Circuit

The CSP signal from U16 goes through a buffer (U3), into a resistor-capacitor circuit to correct width (CR4, R46, R22). U15 then re-shapes the signal before it is split. One path goes through a delay circuit (TP9), into a buffer to produce the CSPD signal (composite sync pulse delayed), which is output at connector J2, pin 11. The second path goes through inverting and edge-sharpening stages, and over to the Black Amplifier circuit. In the Black Amplifier circuit, the CSP signal is buffered and joined with the SUB CBPL signal from the Composite Blanking circuit to form the Black output (TP12) at J8, pin 1.

A branch of the CSP signal from U9 goes to Q4, to develop a clamp pulse at the end of sync. Two resistor-capacitor networks set the width and timing. The burst clamp pulse is buffered (TP9), then is output via pin 9 of connector J2.

9-20 Composite Blanking Pulse (CBP)/Short Composite Blanking Pulse (SCBP) Circuit

The composite blanking pulse (CBP) from U16 goes to U3. Jumper J1 (525/625) plus a resister pair sets the horizontal blanking width of the CBP. The signal re-enters U3 for shaping, is delayed, then goes back for re-shaping, and finally emerges as the composite blanking pulse (CBP) output (TP11), on pin 15 of connector J2.

The CBP signal is also routed from U3 for shaping at U28, then goes to the Black Amplifier circuit as SUB CBPL. Jumper J5 selects NTSC (setup) or PAL (no setup).

The shortened composite blanking pulse (SCBP) is developed from the CBP. A delayed CBP is fed into pin 1 of U5, while an earlier CBP enters on pin 2. The shortened pulse goes from pin 3, through a delay into a buffer. The output SCBP signal (TP10) appears at pin 13 of connector J2.

9-21 Burst Gate Circuit

The signal from the Sync Stripper circuit goes to a gain stage, then a tuned bandpass filter, set with jumpers for NTSC or PAL, which passes the chroma frequencies. Gain is added through a common base amplifier (Q7), then the signal is buffered (Q8) before going into a T-switch.

The composite sync signal is buffered and used to make a burst gate (U17), which turns the T-switch on during burst, to pass chroma. Reference burst appears at TP2. This signal is also used in the Chroma Phase Adjustment circuit. The reference burst is used to saturate Q6 to create a sample burst gate signal, which is used in other circuits.

9-22 Set ID Circuit

The Burst Gate signal goes through a one-shot (U22) which gives a fixed time to the gate. Jumper J12 sets the logic level at high for PAL and low for NTSC. A circuit (U19, U22) generates the SET ID signal to the Sync Generator (U16). At power-up, SET ID sets the Sync Generator up for the correct color frame sequence. During operation, the burst flag pulse from the Sync Generator is compared with the burst flag here, and SET ID resets the Sync Generator to the proper phase if necessary.

The signal from Jumper J12 is also used to create signals PSP1 and PSP1L for every line in NTSC, or every other line in PAL. These signals are used in the Band Pass Filter circuit.

9-23 Field 1 Enable Circuit

The pulse from the Sync Stripper circuit, together with REF CSP signal, enters U12 and U4, where the Field 1 Enable signal is produced. Jumper J4 determines the line rate (525/625). The VRST signal is sent to the Sync Generator, which forces a reset of the vertical interrupt at power-up.

9-24 Chroma Phase Adjustment Circuit

The REF BURST signal from the Burst Gate circuit enters a 90-degree phase shifter, with R10 used to adjust the Chroma Phase. The output passes to U6. A phase lock loop is formed with U14 to set 0, 90, 180, or 270 degrees of phase change, using jumpers J9 and J10 to select amount of phase change. The second part of this circuit sets the Chroma Lock Adjustment (L2), using oscillator Y1/Y2/Y3 (NTSC/PAL/PAL-M), which is selected by jumpers J18-J20. The Chroma Lock Error signal appears at TP3.

9-25 Band Pass Filter Circuit

The Chroma Phase signal (selected by J9 and J10) is split into two signals. One signal goes to a band pass filter, which reshapes the square wave to a sine wave. The signal then enters an output buffer, where it appears as output -U SUB (connector J8, pin 9). This signal is checked at TP18.

The other signal passes through a divide-by-four counter (U14) and enters another band pass filter circuit controlled by the PSP1 and PSP1L signals. The PSP1 and PSP1L signals pass through an emitter-follower stage and enter a T-switch (Q9) which controls the Y SUB signal. R14 adjusts the Y SUB GAIN for the signal. The PSP1L signal also enters another emitter-follower stage, then goes to a second T-switch (Q10) for PAL. R16 adjusts the -V SUB GAIN of this signal. C22 is used to adjust the -V SUB PHASE. The Y SUB and -V SUB signals combine (Q11), then enter a bandpass filter to produce a sine wave. C82 adjusts the phase of this signal. The output (TP17) appears at connector J8 pin 5 as Y SUB, and is also sent to the Black Amplifier circuit (not shown in Figure 9-4).

9-26 Composite Video Timing PWA Test Points, Jumpers, and Adjustments

Table 9-4 lists the test points for the Composite Video Timing PWA, Table 9-5 lists the jumpers, and Table 9-6 lists the adjustment points.

Table 9-4. Composite Video Timing PWA Test Points

Test Point	Signal
TP1	H LOCK ERROR (Horizontal Lock Error Signal)
TP2	REF BURST (Reference Burst)
TP3	CHROMA LOCK ERROR
TP4	GND (Analog Ground)
TP5	REF VIDEO (Reference Video)
TP6	GND (Analog Ground)
TP7	BURST
TP8	CLMP (Burst Clamp)
TP9	CSPD (Composite Sync Pulse Delayed)
TP10	SCBP (Short Composite Blanking Pulse)
TP11	CBP (Composite Blanking Pulse)
TP12	BLACK
TP13	+15V (+12V)
TP14	–15V (–15V)
TP15	GND (Analog Ground)
TP16	GND (Analog Ground)
TP17	V SUB
TP18	–U SUB
TP19	+5V
TP20	Sample Gated Video Signal
TP21	REF CSP (Reference Composite Sync Pulse)
TP22	GND (Analog Ground)

Table 9-5. Composite Video Timing PWA Jumpers

Jumper	Description
J1	Selects 525/625 Line Rate: Position 1-3 (525) Position 4-2 (625)
J4	Selects 525/625 Line Rate: Position 3-1 (625) Position 4-2 (525)
J5	Selects NTSC/PAL: Position 3-1 (NTSC) Position 4-2 (PAL)
J6	Selects Component/Composite: Position 1-3 (Composite) Position 4-2 (Component)
J7	Selects NTSC/PAL: Position 1-3 (NTSC) Position 4-2 (PAL)
J8	Selects Setup/No Setup: Position 1-2 (No Setup) Position 4-3 (Setup)
J9, J10	Selects Phase Difference: J9, Position 3-1 (180 Degrees) J9, Position 4-2 (270 Degrees) J10, Position 3-1 (0 Degrees) J10, Position 4-2 (90 Degrees)
J11	Selects NTSC/PAL: Position 1-4 (NTSC) Position 3-2 (PAL)
J12	Selects NTSC/PAL: Position 3-1 (PAL) Position 4-2 (NTSC)
J13	Selects 525/625 Line Rate: Position 3-1 (525) Position 4-2 (625)

(Continued next page)

Table 9-5. Composite Video Timing PWA Jumpers (Continued)

Jumper	Description
E1/E2	Selects Y1 (NTSC) Oscillator
E3/E4	Selects Y1 (NTSC) Oscillator
E5/E6	Selects Y2 (PAL) Oscillator
E7/E8	Selects Y2 (PAL) Oscillator
E9/E10	Selects Y3 (PAL-M) Oscillator
E11/E12	Selects Y3 (PAL-M) Oscillator

Table 9-6. Composite Video Timing PWA Adjustment Points

Point	Description
L1	H LOCK ADJ — Horizontal Lock Adjustment
DS1	H LOCK LED (Green) — Horizontal Lock Indicator
L2	CHROMA LOCK ADJ — Chroma Lock Adjustment
R7	H PHASE ADJ — Horizontal Phase Adjustment
R10	CHROMA PHASE ADJ — Chroma Phase Adjustment
R14	Y SUB GAIN
R16	-V SUB GAIN
R18	BURST AXIS
R19	BURST GAIN
R20	BURST NULL
C22	-V SUB PHASE
C82	Y SUB OUT

SECTION 10

DUMPSTER BUS INTERFACE PWA

10-1 GENERAL DESCRIPTION

The Dumpster Bus Interface PWA (P/N 1430956) links the AT computer bus with the switcher control bus (known as the "Dumpster" bus), to pass data back and forth. This data is transferred as a series of data-and-address byte pairs. The address bytes are switcher addresses, but they are data bytes on the AT bus, bits 8 through 15. When passed to the switcher, data bits 8 through 15 become the address bytes for switcher functions. The RAM on this PWA is loaded and unloaded on command from the main CPU, without burdening the CPU with separate transfer operations. Figure 10-1 shows the Dumpster Interface Bus PWA, and identifies its main components, test points and connectors.

The Dumpster Bus Interface PWA views the AT bus as a collection of five I/O address locations (hex): 360, 362, 363, 364, and 365.

- Location 360 is a read/write address for the switcher or Dumpster bus data-address pairs. Each pair contains an address location and a data byte, forming a 16-bit word.
- Location 362 is a write-only address pointing to a specific location in local RAM that contains the switcher address.
- Location 363 is a read-only address containing status information for the main CPU.
- Location 364 is a write-only address controlling the Start Dump command.
- Location 365 is a write-only address controlling the Clear Dump command.

All address locations are eight-bit ports except Location 360, which is 16-bits. The data-address pair bytes that are fed to the static RAM on the Dumpster Bus Interface PWA mirror locations on the Dumpster bus in the switcher. The high bit of the address pair (bit 15) is the read/write bit, which allows data to be read out from the Dumpster bus, or data to be sent to the bus.

To start a dump cycle, the following sequence of events takes place:

- Data is written in location 364 (Start Dump command). This command starts the count in the state machine for the number of data-address pairs being transferred in this particular dump operation.
- Location 363 is monitored by the main CPU to ensure Dumpster is not busy.
- The address bits and data bits are combined to form a 16-bit word, with address bits in high byte. This word is written to location 360.
- An address is written to location 362, forming an address pointer to the 16-bit word.

When the Dump is done, a Clear Dump instruction is sent to location 365.

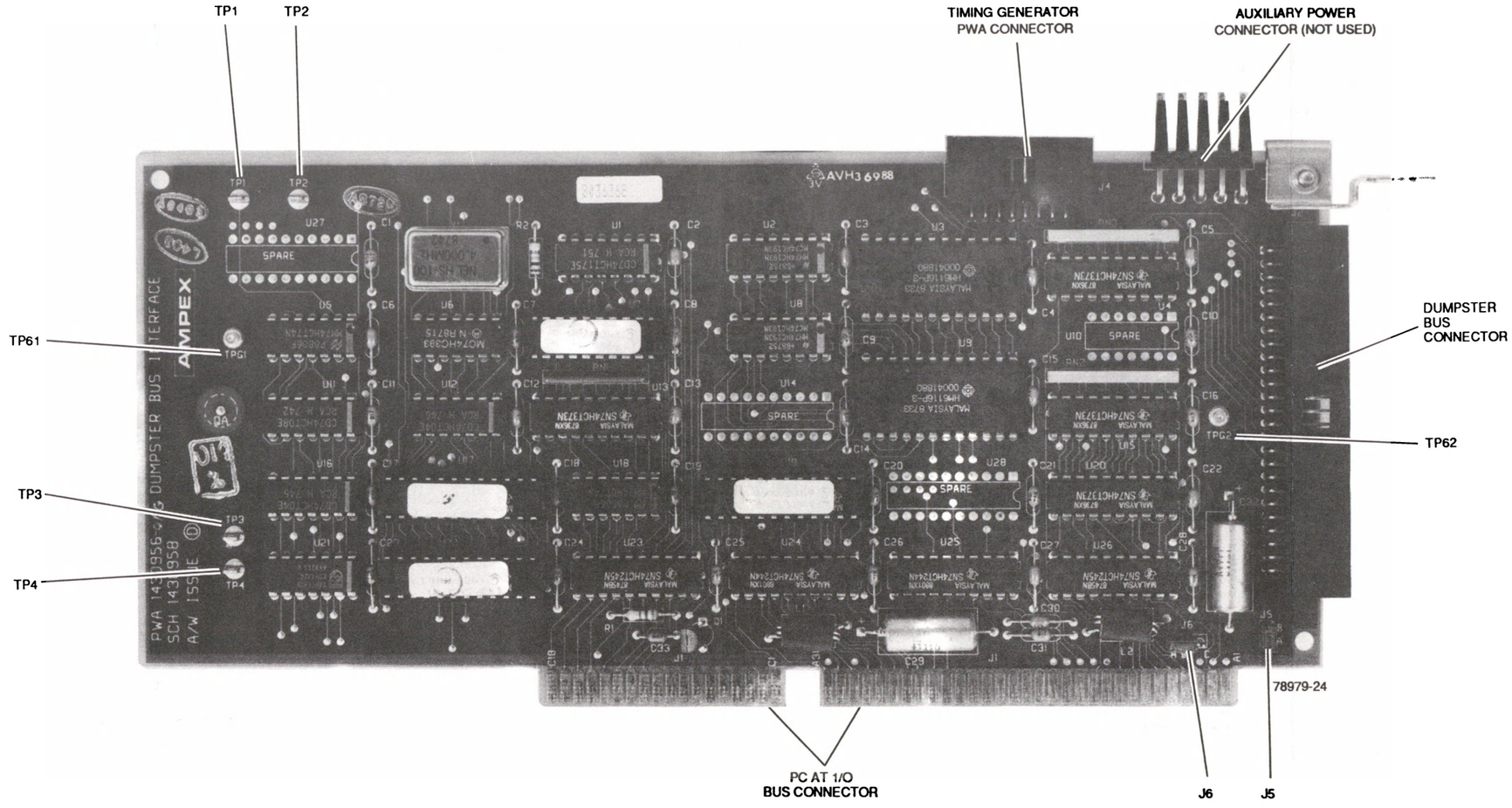


Figure 10-1.
Dumpster Bus Interface PWA

10-2 THEORY OF OPERATION

Figure 10-2 presents a block diagram of the primary functions on the Dumpster Bus Interface PWA. The PC AT bus drivers and receivers (U23, U24, U25, U26) are connected to the PC AT bus slot connector J1. The state machine (U1, U6, U7) consists of a PAL, counter, and latch that are driven by a 4.0 MHz oscillator (Y1). This state machine produces a down counter clock, which is used to control the passing of data back and forth between the buses. The Long Count signal is used to extend the cycle from 4 microseconds to 8 microseconds. When a Start Dump command is decoded from the PC bus, the Busy latch (U5, pin 9) is set, and the Busy signal is detected by the state machine, and also by the Busy Logic (U5, U11, U16) and Function Control PALs. This Busy signal appears at TP1 as a low when true. At the end of the busy time (i.e., when all data has been passed to or from the Dumpster bus), the other half of U5 generates a terminal count signal. The Busy Logic also receives the Start Dump (364 hex) and Clear Dump (365 hex) signals from the function control PALs.

The Address Decode PAL (U19) decodes addresses and commands from the AT bus, sending them to the Functional Control PALs and the Load/Unload Counter (U2, U8). The address load signal appears at TP3, which signals the start of a load operation. The Load/Unload Counter is filled directly from the AT bus receivers, and counts down using the down counter clock of the state machine. During an unload operation, the data bytes go to the Data Byte RAM (U9), and the address bytes go to the Address Byte RAM (U3).

The Function Control PALs (U17, U22) receive control signals from the Address Decode PAL, and send bus control signals to these locations:

- AT bus
- Busy Logic on the Dumpster Bus Interface PWA
- Switcher (Begin Strobe at TP2)
- Read/write signals to the Data Byte RAM and Address Byte RAM

The Address Byte RAM (U3) and the Data Byte RAM (U9) are loaded from the Load/Unload Counter and the AT bus. During the unload cycle, the address byte data comes out of U3, through latch U4, to the address byte section of the Dumpster bus interface (J2). TP4 displays the Dumpster Address Enable signal. The Data Byte RAM (U9) data passes through latch U20 to the Dumpster bus. The data is transferred from the Dumpster bus to the switchers. Return data goes through U15, over the data byte lines (J2, pins 37 to 47) to the internal bus. The bus transfers the data to U26, which is connected to the AT bus. The 80286 CPU receives the data from the AT bus.

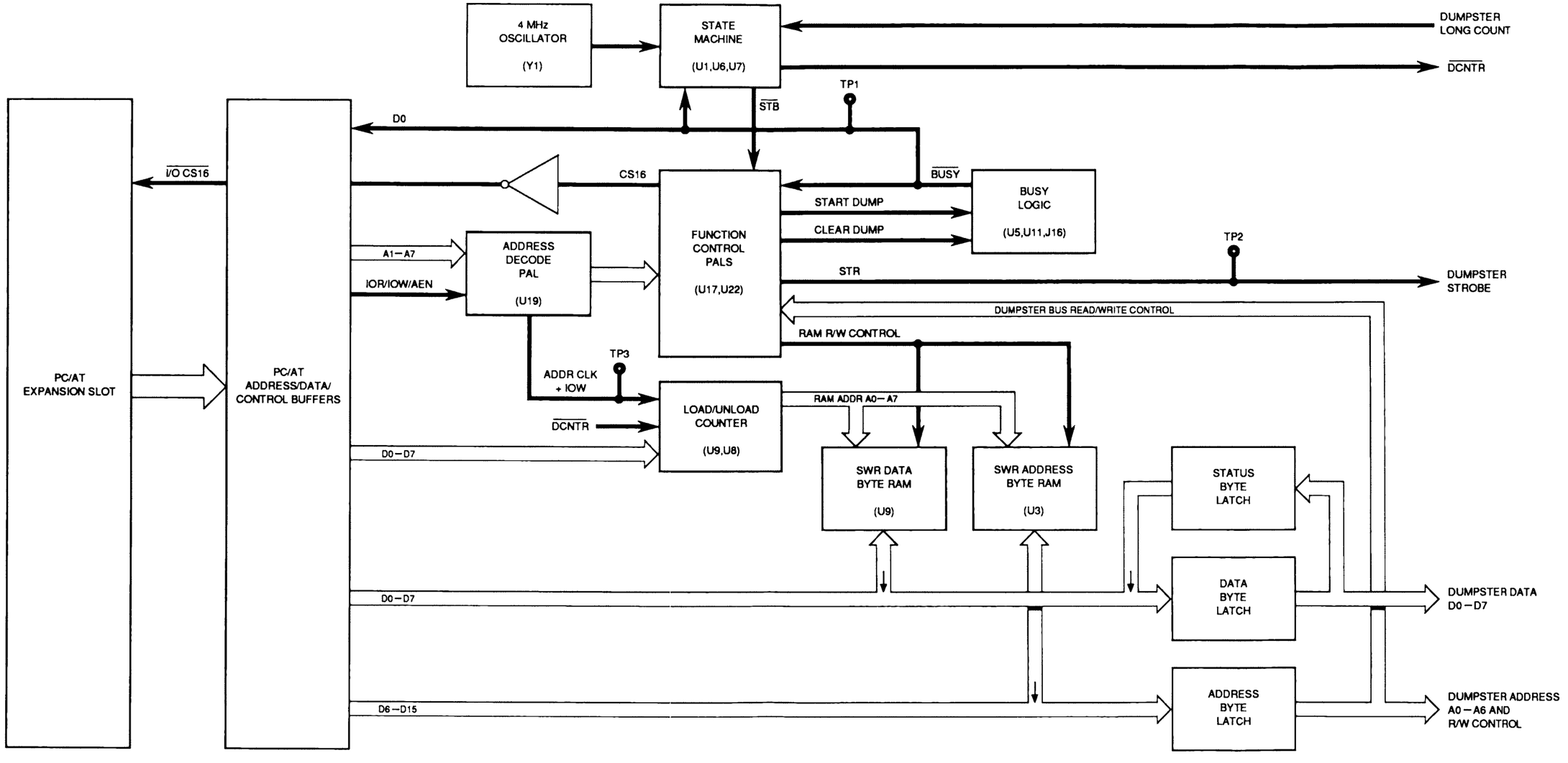


Figure 10-2.
Dumpster Bus Interface PWA
Block Diagram

10-3 TEST POINTS AND JUMPERS

Table 10-1 lists the test points and jumpers for the Dumpster Bus Interface PWA.

Table 10-1. Dumpster Interface Bus PWA Test Points and Jumpers

Test Point	Signal	Description
TP1	Low = TRUE	-BUSY
TP2		DSTR (Dumpster Strobe)
TP3		ADDR CLOCK + IOW (Address Clock and I/O Write)
TP4		Dumpster Address Enable
TPG1		Digital Ground
TPG2		Digital Ground
Jumper	**Position**	
J5	AB (IN)	Connects Digital and Analog Grounds
J6	AB	Factory Setting (Normal)
J6	AC	Selects +5V from auxiliary power converter (Not Used)

SECTION 11

8-CHANNEL ILC PWA

11-1 GENERAL DESCRIPTION

The ILC (Intelligent Line Controller) PWA (P/N 1431025) is a communication controller based on an 80C186 CPU, which supports up to eight RS-422 channels. The ILC PWA controls devices such as VTRs and external switchers which are connected to the ACE 25 editing system. Figure 11-1 shows the ILC PWA and identifies key components. Primary features of the 8-Channel ILC PWA are:

- Local CPU (12.5 MHz 80C186 processor)
- Local ROM (16 Kbytes, expandable up to 128 Kbytes)
- Shared RAM (16 Kbytes, expandable up to 64 Kbytes)
- 8-Channel UART (for RS-422)
- Host Register
- Arbitration Logic for Shared RAM

A number of ICs on this PWA are socketed for easy replacement. Appropriate care to avoid static electricity discharge is necessary when handling the 8-Channel ILC PWA.

11-2 Local CPU

The 80C186 CPU is a 12.5 MHz version of the 80C186 microprocessor, with integrated support to minimize additional support circuitry. The CPU has 20-bit addressing capability, with multiplexed address/data lines. It controls all devices connected to the local bus, and the dual-ported RAM. The main operating program for the 80C186 is stored in local ROM, with additional driver information for external devices stored in local RAM.

The 80C186 local CPU performs numerous functions, including:

- Service all eight RS-422 channels. Each channel can interrupt CPU, or alternatively, CPU can disable interrupts and poll each channel for service.
- Service all devices attached to RS-422 ports by executing device driver routines.
- Communicate with AT CPU through shared RAM. Data and commands are passed from one CPU to the other through this shared RAM .
- Run board diagnostics to check integrity of memory and communication ports.

All address/data decoding operations are done by the local CPU.

11-3 Local RAM

The ILC PWA contains 16 to 192 Kbytes of local RAM in socketed static RAM chips (U18-U23). Available memory is selected with jumpers J01, J02, and J03; some sockets may not be used. This local ram contains the device drivers and operating system software for the 8-Channel ILC PWA (except for the AMON monitor and diagnostics). The software in the local RAM is downloaded through the shared RAM area by the main CPU.

11-4 Local ROM

Local ROM is contained in two IC sockets (U1 and U2), and can be extended up to 128 Kbytes total. Jumpers J02 and J03 are used to select available memory size. The local ROM contains the AMON monitor and diagnostics routines for the local CPU. The AMON monitor starts the task of downloading the operating system software into local RAM by the local CPU. The diagnostics routines check the local RAM, the shared RAM, and all I/O ports in loopback mode.

11-5 Shared RAM

The local CPU and host CPU communicate with each other through 16 Kbytes of shared RAM, expandable to 64 Kbytes. An arbitration circuitry is responsible for conflict resolution when both CPUs try to access memory at the same time. This shared RAM consists of two static RAM chips (U20, U30), with jumpers J12, J13 and J14 used to select capacity. Shared RAM is addressed using two address segments (low byte and high byte) that are determined by the address multiplexer. The data for the shared RAM goes through a pair of address buffers: one for the 80C186 and the other for the 80286. Typically, data is stabilized for one clock cycle before it is sent out; however, if access is changed from one CPU to the other, more wait time is required.

11-6 8-Channel UART

All eight RS-422 ports communicate with the local CPU through the eight-channel UART. Host CPU can write into an output port for two purposes: (1) to reset the local CPU; and (2) to set the shared memory address. The UART has full RS-232 communications available on all channels; however, only RS-422 functions are used. All voltages are TTL-level; no differential lines exist. An internal loop-back function in the UART allows diagnostic testing by the local CPU on power-up or reset. Each channel in the UART can be set independently for baud rate and other characteristics, using system software.

11-7 Arbitration Logic

The arbitration logic controls access to the shared RAM by the local CPU and host CPU. The logic is embedded in a PAL (U11) that functions as a state machine. The arbitration logic works as follows:

- The 80C186 is assigned state Ready 1, and the 80286 is assigned state Ready 2; in each state, there is no change if no access request is made.
- If access request is from current state CPU, access is granted with no wait states or lost cycles. Wait states occur only when the 80C186 accesses shared memory during Ready 2, or the 80286 accesses shared memory during Ready 1.
- Current state is disabled, then changed to the other state, with one wait cycle used to stabilize data.

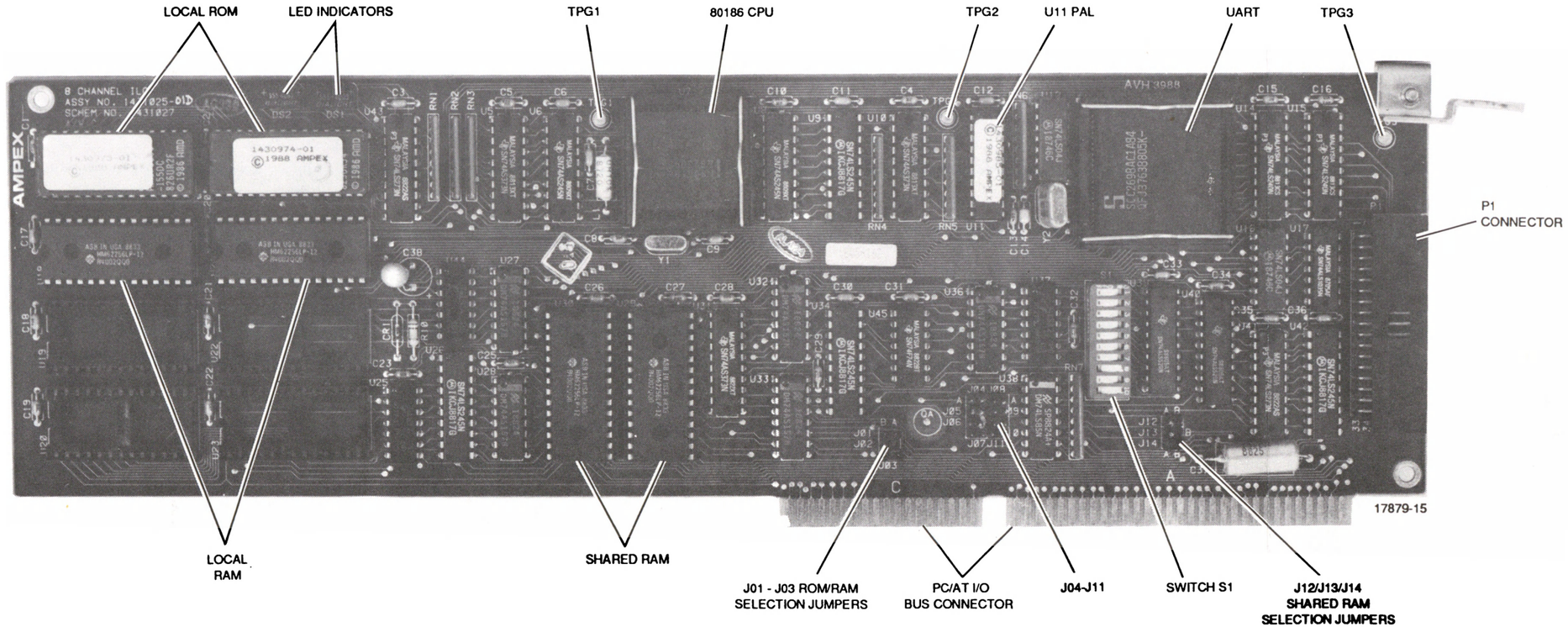


Figure 11-1.
8-Channel ILC PWA

11-8 PC AT Bus Connection

The ILC PWA is connected to the PC AT bus through the bus slot. The shared RAM area and the Host Register is seen by the 80286 main CPU via this bus connection. The connection also supplies power and ground to the ILC PWA.

11-9 THEORY OF OPERATION

The following paragraphs present a brief theory of operation for each major area of the 8-Channel ILC PWA. Figure 11-2 is a block diagram of the 8-Channel ILC PWA that shows the bus structure and key functional elements of this PWA.

11-10 Local CPU

The 80C186 derives its clock frequency (divided by 2) from oscillator Y1. The reset line is connected to the master reset for ACE 25, and the power-on reset; the 80286 CPU can also trigger a reset. The non-maskable interrupt (NMI) is currently not used (set via jumpers J4-J11). Four other interrupt lines of the CPU are connected to the UART. Data/Address lines AD0-AD15 are multiplexed; four other address lines are used separately. The local CPU can use either 8-bit or 16-bit words, divided into low-byte and high-byte segments. It also has lines to enable the address latch (ALE), read and write, plus assorted control lines. A restart line is connected to the UART and local bus. The CPU uses address latches U5 and U10 to set addresses for local RAM, and buffers data through bus drivers U6 and U10.

11-11 Local Bus

The local bus is used for address, data, command and status information, with multiplexed address-data lines. During the first part of a cycle, the line is used for addressing; during the second part, the line is used for data. Addresses are latched, while the data is buffered, during alternate periods. The address bus connects the local CPU, the local RAM, the local ROM, the UART, and the multiplexer for the shared RAM. Jumpers J2 and J3 are used to enable the last two bits of addressing for the local ROM and RAM, when available. The data bus connects the local CPU, the local RAM, local ROM, the UART, and the arbitration logic. The command bus transfers commands such as read/write, ROM select, and other control signals, from the local CPU to the local RAM, local ROM, the UART, and the arbitration logic. The status bus is used for interrupt lines and ready lines, linking the local CPU to the UART. The ready line is also used by the arbitration logic to signal completion of read/write cycles and access to the shared RAM.

11-12 Interrupts

There are two interrupt mechanisms used in ILC communications with the host. The first is the ILC interrupt to the host. This is done by the 80C186 CPU accessing an I/O location within its I/O space. This interrupt signal is jumper selectable (J04-J07) and can be programmed to connect to any four of the host's interrupt lines. The second mechanism is the Color Framer Board (CFB) interrupt to the ILC. The Color Framer Board interrupts the ILC and host at every field. This interrupt is connected to the NMI line of the local CPU. The interrupt signal is jumper selectable (J08-J11) and can be programmed to connect to any four of the host's interrupt lines.

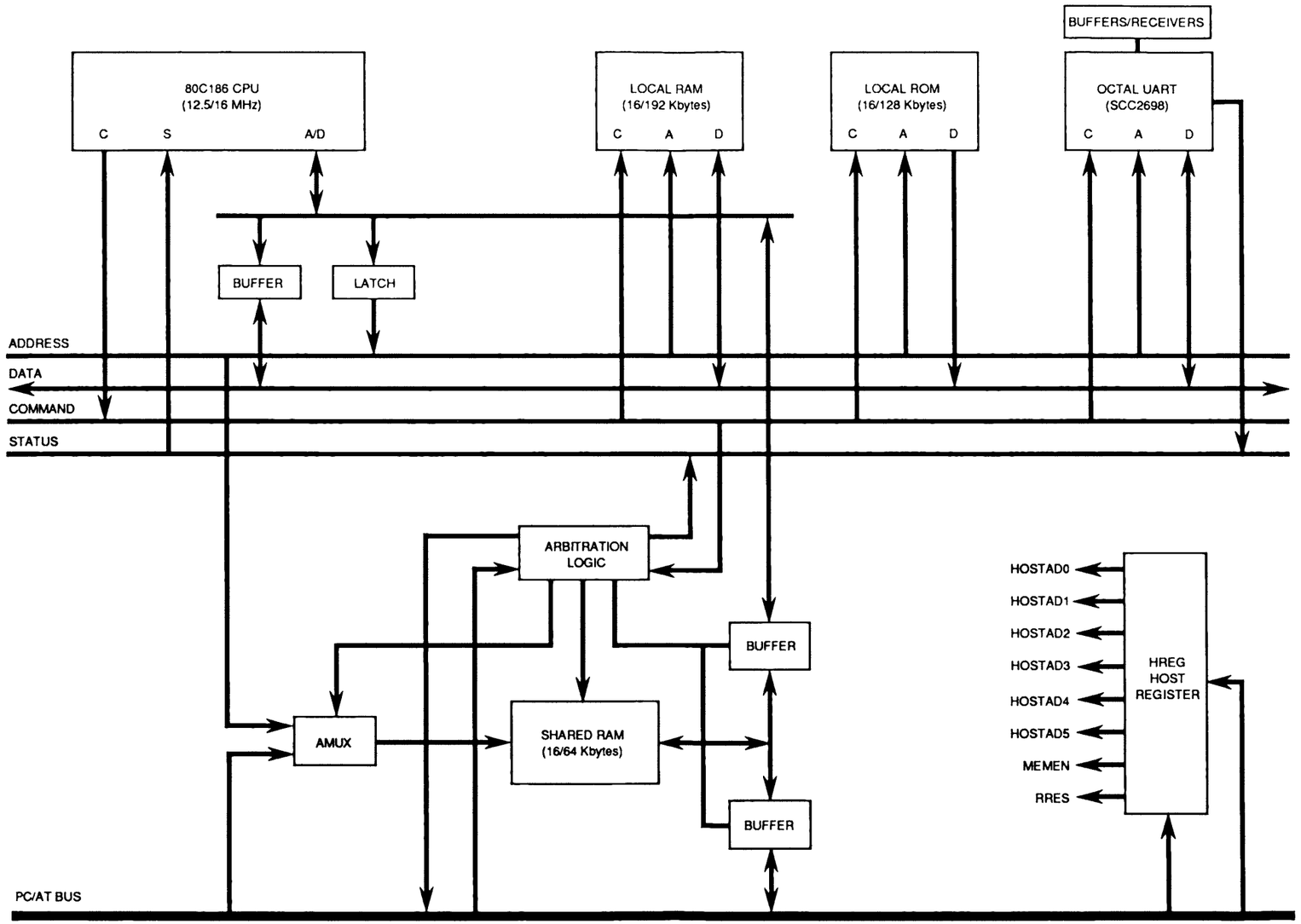


Figure 11-2.
8-Channel ILC PWA Block Diagram

11-13 Host Register

Host register (U41) is shown as HREG in the block diagram. The register location is set by switch S1. A comparator (U38 and U39) compares the AT address to the switch. Data is clocked into U41, and buffered through U40 before going to the PC AT bus. A memory enable line (MEMEN) enables or disables the comparator, to enable/disable memory select. The register is also linked to the reset line (RES), controlled by the host, to trigger a reset of the ILC PWA and local CPU.

11-14 Arbitration Logic

The arbitration logic receives commands from the local CPU on the local bus. Address information is loaded into a multiplexer system (AMUX), consisting of four address multiplexers (U27, U28, U32, U33), and a read/write enable multiplexere (U36). Host CPU information is also loaded into this multiplexer system. The arbitration logic controls the AMUX, regulating the shared RAM area, in conjunction with controlling two data buffers. One buffer (U9, U36) stores local CPU data, while the other buffer (U42, U34) stores host data. These buffers are linked to the shared RAM to exchange data.

11-15 UART

Oscillator Y2 supplies the clock signal to the UART. Local address/data lines are connected to LAD1-LAD6; lines BD0-BDB7 are also used. Control lines for the UART go to the local CPU, plus four interrupt lines. The UART receives signals from outside devices through a buffer-driver (U14) from connector P1. The UART transmits signals through buffer-driver U16 to connector P1, to reach outside devices.

11-16 TEST POINTS, JUMPERS, SWITCHES, AND LEDS

Information on the test points, jumpers, switches and LEDs on the 8-Channel ILC PWA is presented in the following paragraphs.

11-17 Test Points

The 8-Channel ILC PWA has three test points (TPG1, TPG2, and TPG3), that display the digital ground signal.

11-18 Jumpers

Memory size is selectable with jumpers, as shown in Table 11-1.

Table 11-1. 8-Channel ILC PWA Memory Selection Jumpers

Jumper	Position	Description
J01	IN	32K x 8 EPROM
J0	OUT	
J03	IN	32K x 8 RAM (Local RAM)
J04	OUT	
J05	OUT	
J06	OUT	
J07	OUT	
J08	OUT	
J09	OUT	
J10	OUT	
J11	OUT	
J12	OUT	32K x 8 RAM (Shared RAM)
J13	OUT	32K x 8 RAM (Shared RAM)
J14	IN	32K x 8 RAM (Shared RAM)

11-19 Switches

Switch S1 must be set to 280 (Hex) as shown in Figure 11-3. This setting defines the I/O port address used by the 80286 CPU to access the shared RAM on the 8-Channel ILC PWA.

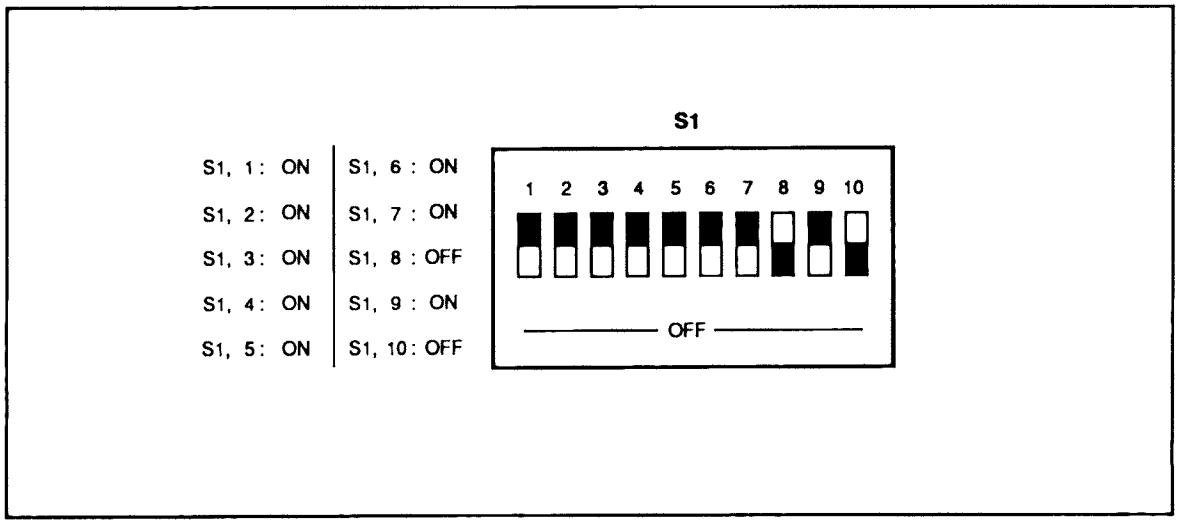


Figure 11-3. 8-Channel ILC PWA Switch Settings

11-20 LEDs

The LEDs (DS1 and DS2) are used to display information on the operational status of the ILC PWA. The LEDs are connected to a register (U43) which is controlled by the 80186, using software in local ROM. When reset or powered on, the LEDs will first blink, then remain on if the RAM, ROM, and UART are operational.

11-21 ILC PWA STARTING DIAGNOSTICS

The two LEDs (DS1, DS2) display diagnostic information whenever the ILC PWA is reset, either at power-on or through a reset command from the 80286 main CPU. The diagnostic sequence begins with all LEDs flashing on. This initial flash appears only when power is first applied; during a 80286 system reset, the LEDs are normally already on. If the LED sequence stalls during the opening diagnostic sequence, the following problems may have occured:

- ROM failure
- 80C186 CPU failure
- Catastrophic ILC PWA board failure

To correct problem, first replace the local ROMs (U1, U2), and power on equipment again. If this does not solve the problem, replace the 80C186 CPU (U7), and power on equipment again. If this, too, does not solve the problem, and as a final resort, replace the ILC PWA board, and power on equipment again. A catastrophic board failure is extremely unlikely to occur.

The UART test begins after the RAM test is complete. The LEDs light sequentially as the eight channels are tested. If a stall occurs, replace the UART (U13). No channel-specific repairs are possible. The external line drivers and cables cannot be tested without special equipment. The startup diagnostics are complete when all LEDs light again.

If the I/O port address on switch S1 (see paragraph 11-19) is set wrong, the ACE 25 monitor will display the DOS Error Return Code 1 (DOS ERC 1). To validate the DOS Error Code 1, the following procedure is used:

1. Format a DOS system disk.

2. Copy file ILC.EXE to DOS system disk from an ACE 25 system disk.

3. Create a test program on the test disk, using the following DOS commands:

   copy con: autoexec.bat (RETURN)

   @echo off (RETURN)

   ilc (RETURN)

   if error level 1 echo No Response from ILC (RETURN)

   (Control)-Z (RETURN)

Insert this test disk into the ACE 25, and power on again. If the ILC Worm banner is displayed, but no error message appears within 15 seconds, the ILC PWA is working correctly.

SECTION 12

INPUT/OUTPUT PWA, SWITCHER BACKPLANE PWA, AND SWITCHER EXTENDER PWA

12-1 INTRODUCTION

This section covers three different boards: the Input/Output PWA (I/O PWA), the Switcher Backplane PWA, and the Switcher Extender PWA.

12-2 INPUT/OUTPUT PWA

The Input/Output PWA contains circuitry and connectors for interfacing the ACE 25 system with external devices. The following paragraphs describe the I/O PWA and provide guidelines for troubleshooting.

12-3 General Description

The Input/Output PWA (P/N 1431457) is attached to the inside rear panel of the Edit Controller chassis. It is mounted on extension posts located among the input and output connectors, which are soldered to the PWA and attached to the metal rear panel. Key components on this board are identified in Figure 12-1.

The Input/Output PWA has four primary functions:

- Receive reference video input, loop it, and pass signal to Color Field Detector PWA.
- Receive video and sync signals from Video Display PWA and drive two data monitor outputs.
- Receive input signals from devices connected to the eight ILC connectors on rear panel.
- Transmit output signals to ILC devices from 8-Channel ILC PWA.

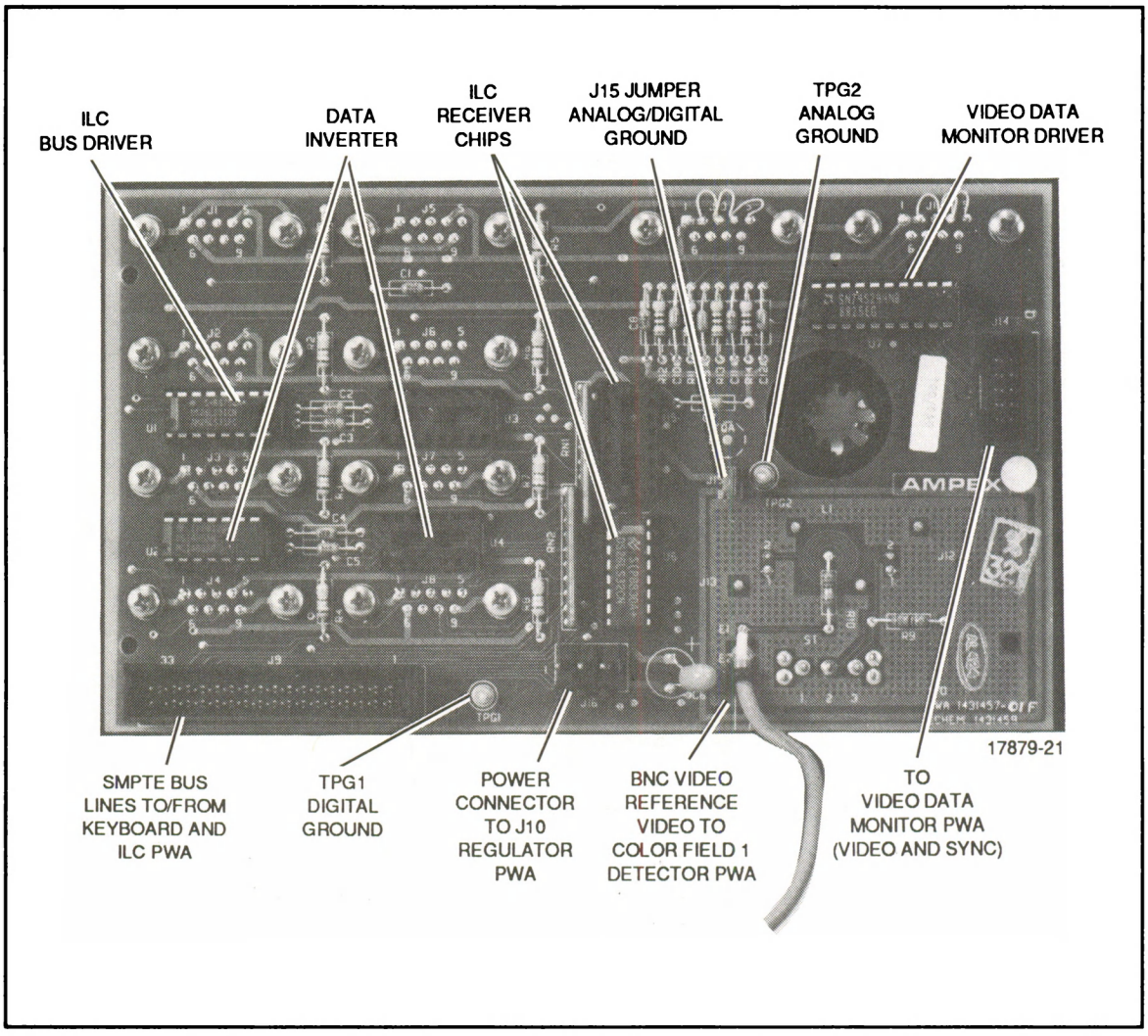


Figure 12-1. Input/Output PWA

Figure 12-2 shows a block diagram of the Input/Output PWA.

12-4 Troubleshooting

Active IC components on the Input/Output PWA are mounted in sockets for convenient replacement. If communication with any external device connected to the ILC channels is faulty, the socketed ICs should be checked. One method to check the ILC bus drivers and receivers is to switch the chips in each pair (U1/U3), (U2/U4), and (U5/U6). If communication is still faulty, check the 8-Channel ILC PWA.

The connectors on the rear panel of the Edit Controller unit that are attached to the Input/Output PWA contain no active components. Cables linking the ACE 25 to external equipment should be checked whenever communication faults develop.

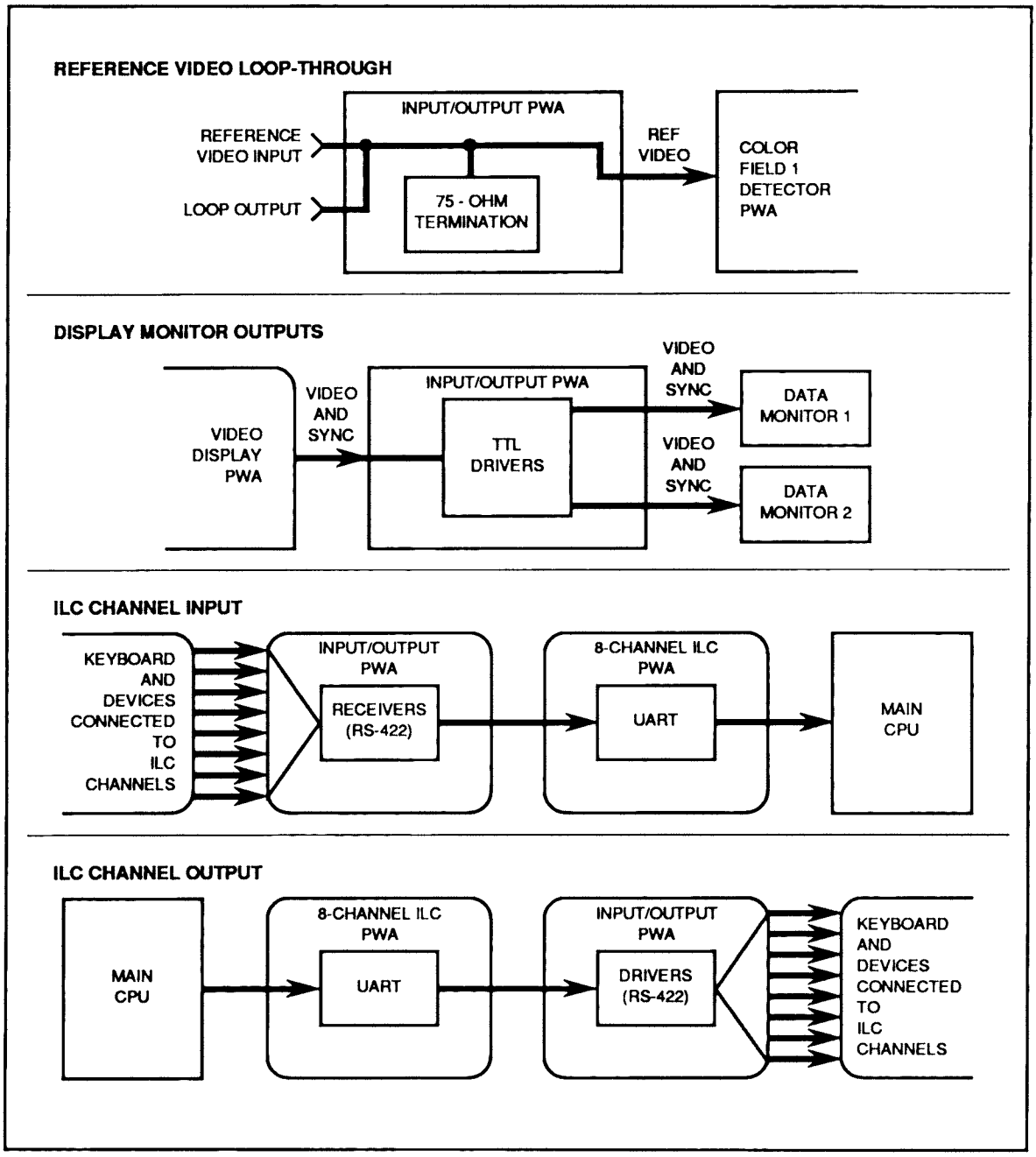


Figure 12-2. Input/Output PWA Block Diagram

12-5 SWITCHER BACKPLANE PWA

The Switcher Backplane PWA is an optional PWA that is used in ACE 25 systems containing internal audio and/or video switchers. The following paragraphs describe this PWA.

12-6 General Description

The Switcher Backplane PWA (P/N 1445917) is attached to the lower rear panel of the ACE 25 Edit Controller unit. Video and audio input and output connectors are mounted directly on one side of the PWA; switcher backplane connectors are mounted on the other side. The switcher backplane has no active components. It transfers Dumpster bus data to and from the video and audio switchers, and supplies power to the internal switchers. Figure 12-3 shows the Switcher Backplane PWA with its connectors. A single version of the backplane is used for both component and composite switchers; for composite switchers, only the Y Channel and Key Channel portions of the Dumpster bus are used.

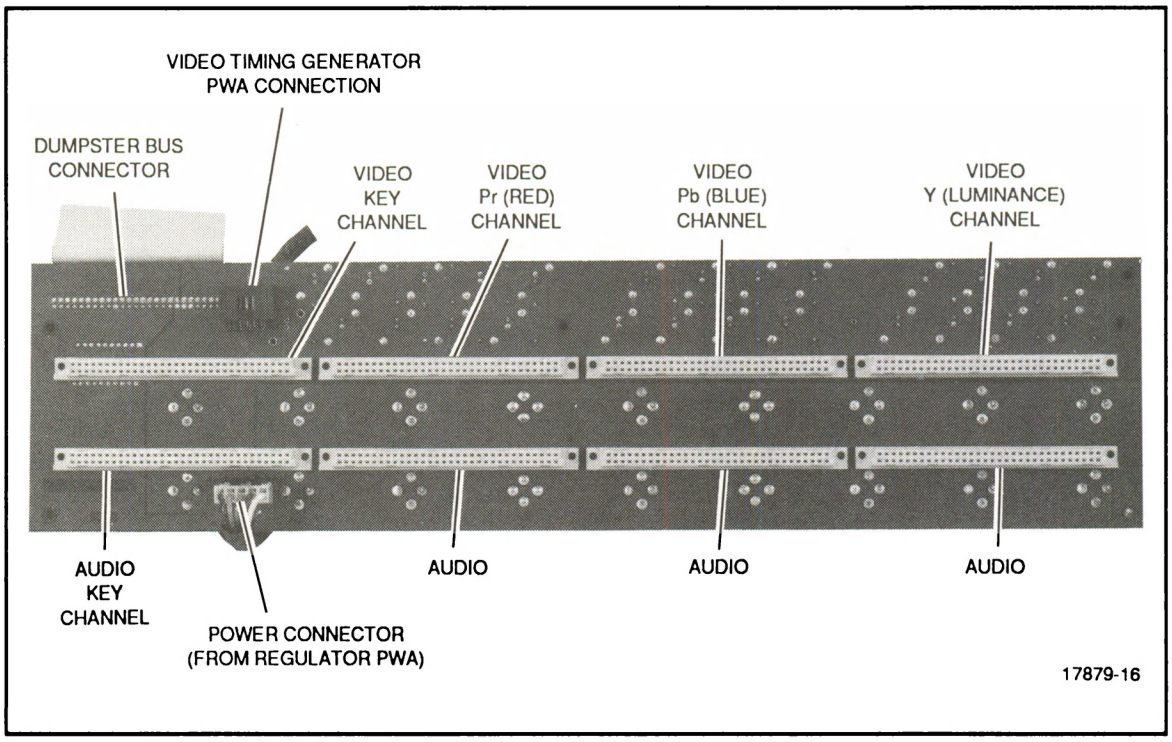


Figure 12-3. Switcher Backplane PWA

12-7 Ground Connections

The ground connections on the Switcher Backplane PWA (analog and digital) are separated by 10k ohms of resistance to reduce noise. The chassis ground is also kept separate from the other grounds for noise reduction.

12-8 Connections

Table 12-1 lists the Switcher Backplane PWA connectors and their function.

Table 12-1. Switcher Backplane PWA Connectors

Connector	Description	Destination
J14	50 Position	Dumpster Bus Interface PWA
J28	10 Position	Video Timing PWA
J46	5 Position, Power	Regulator PWA (J4)
XA1-J1	64 Position	Video Switcher, Key Channel
XA1-J2	64 Position	Video Switcher, Pr (Red) Channel
XA1-J3	64 Position	Video Switcher, Pb (Blue) Channel
XA1-J4	64 Position	Video Switcher, Y (Luminance) Channel
XA2-J1	64 Position	Audio Switcher
XA2-J2	64 Position	Audio Switcher
XA2-J3	64 Position	Audio Switcher
XA2-J4	64 Position	Audio Switcher

12-9 EXTENDER PWA

The Extender Board (P/N 1431596) is used to extend either the audio or video internal switcher boards, so components on the switchers can be accessed. Figure 12-4 depicts the Extender PWA. This board contains no active components which can be serviced.

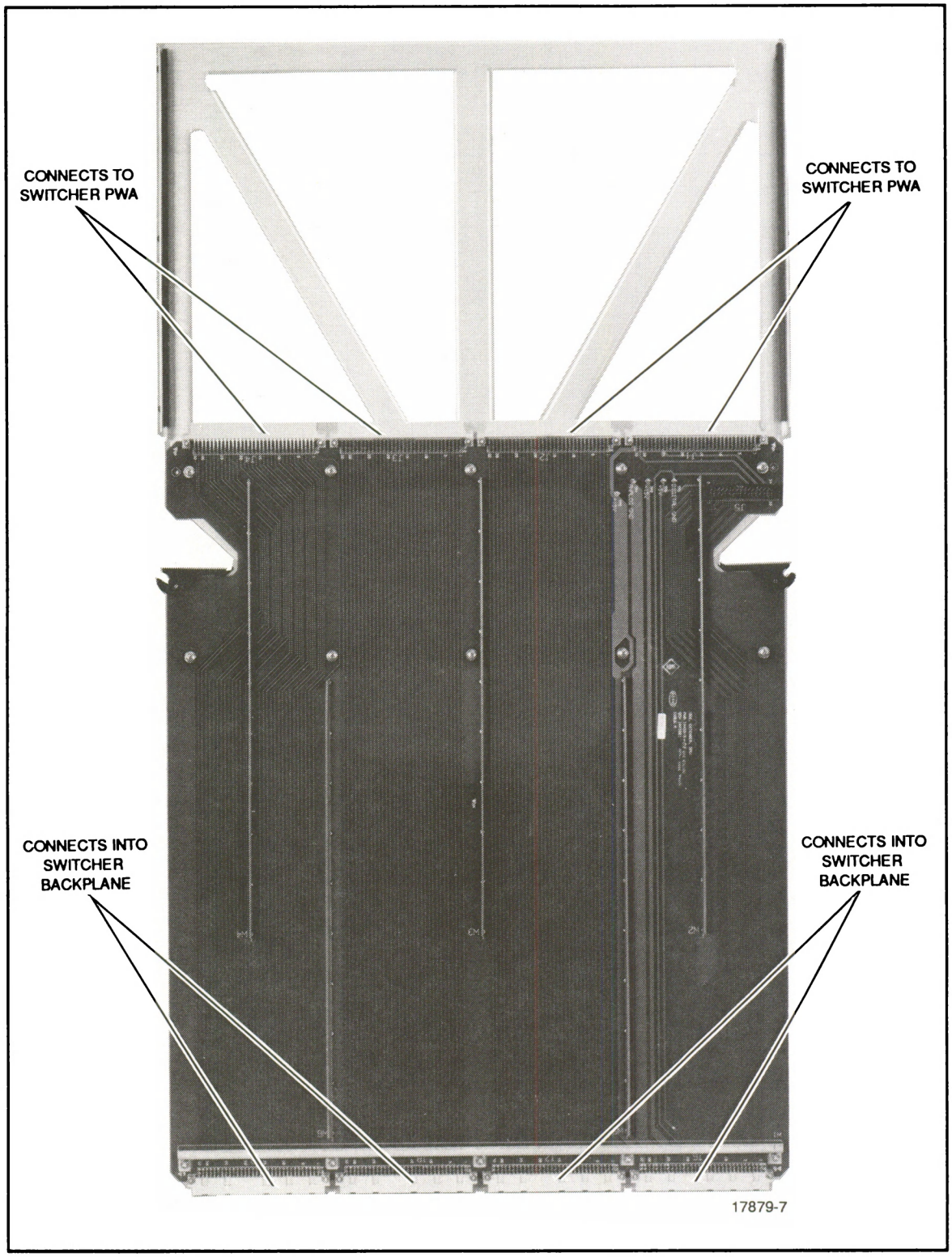


Figure 12-4. Switcher Extender PWA

SECTION 13

COMPOSITE VIDEO SWITCHER PWA

13-1 INTRODUCTION

The Composite Video Switcher PWA (P/N 1443400) is an internal video switcher for composite analog video signals. This PWA plugs into the Switcher Backplane PWA, with four 64-pin connectors providing power and signal connections. External input and output connections are located on the lower rear panel of the Edit Controller unit. An extension board is available for test and adjustment procedures. Figure 13-1 shows the Composite Video Switcher PWA and identifies fuses, jumpers, and adjustment points.

13-2 THEORY OF OPERATION

The following paragraphs describe theory of operation for the Composite Video Switcher PWA and its primary circuits. Figure 13-2 is a diagram showing the main video signal paths on the Composite Video Switcher PWA.

13-3 General Description

The Black video signal is internally generated on the Video Timing PWA from the reference video signal supplied to ACE 25. Six external video signal inputs enter the switcher through the Switcher Backplane PWA from the BNC connectors mounted on the Edit Controller rear panel. An external key video signal input comes to the switcher in the same manner. A clamp signal from the Video Timing Generator PWA is used by the switcher to process the video signals.

The Black input, six external inputs, and the external key input pass through clamping and buffering circuits (shown as triangles labelled "CBC" in Figure 13-2). The clamp signal is generated by the Video Timing Generator PWA as mentioned earlier.

The Black input and six external inputs pass through the clamp stage to the crosspoint bus stage, which has four levels: Black, A Bus, B Bus, and Insert Bus. The Black level is not a complete crosspoint bus, because it only has the Black video signal. This Black level passes through a delay stage into a phase-shifting, clamp-buffer circuit (shown as a triangle labelled "ΦSC"), before entering the Black multiplier circuit.

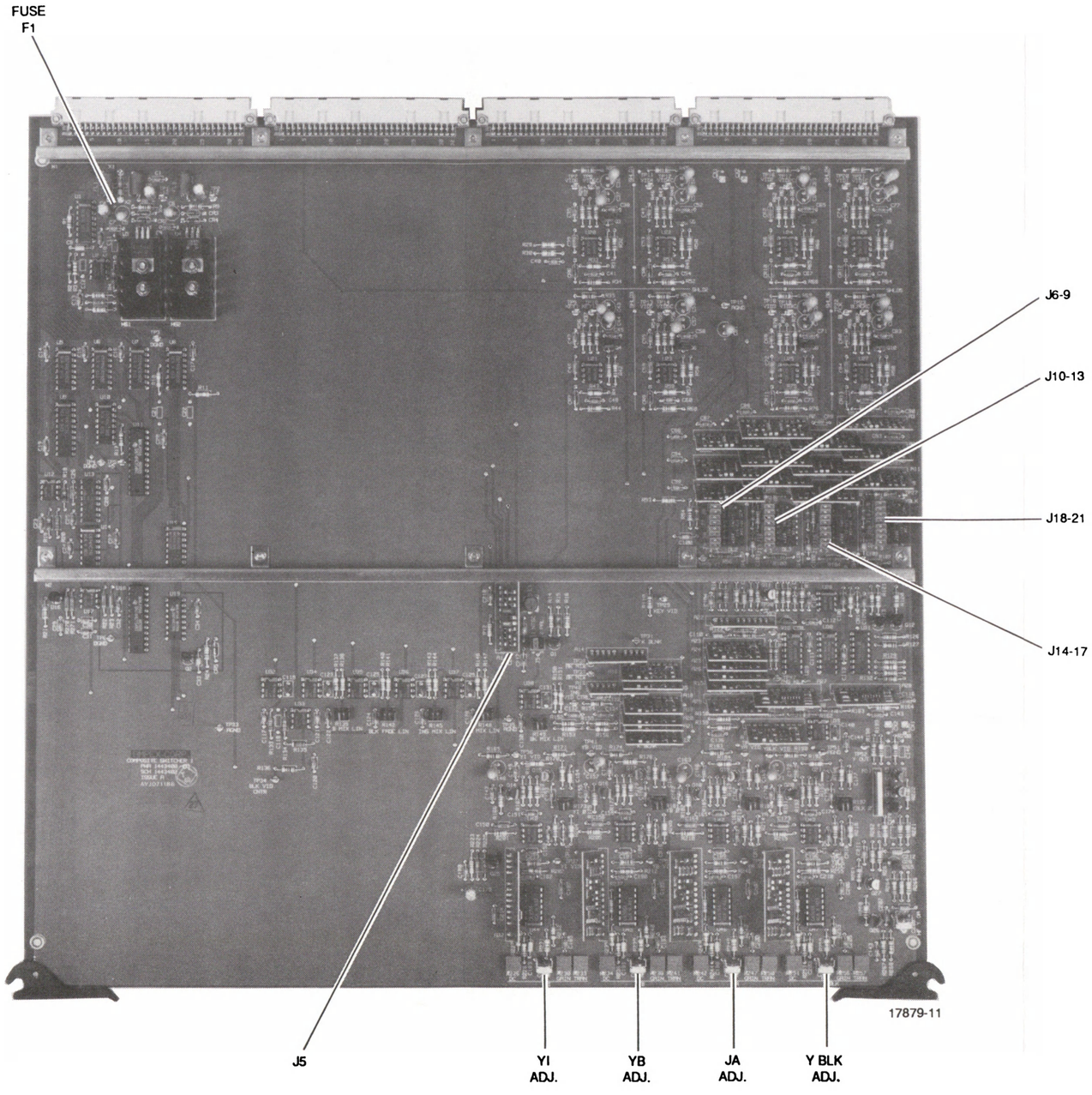


Figure 13-1.
Composite Video Switcher PWA

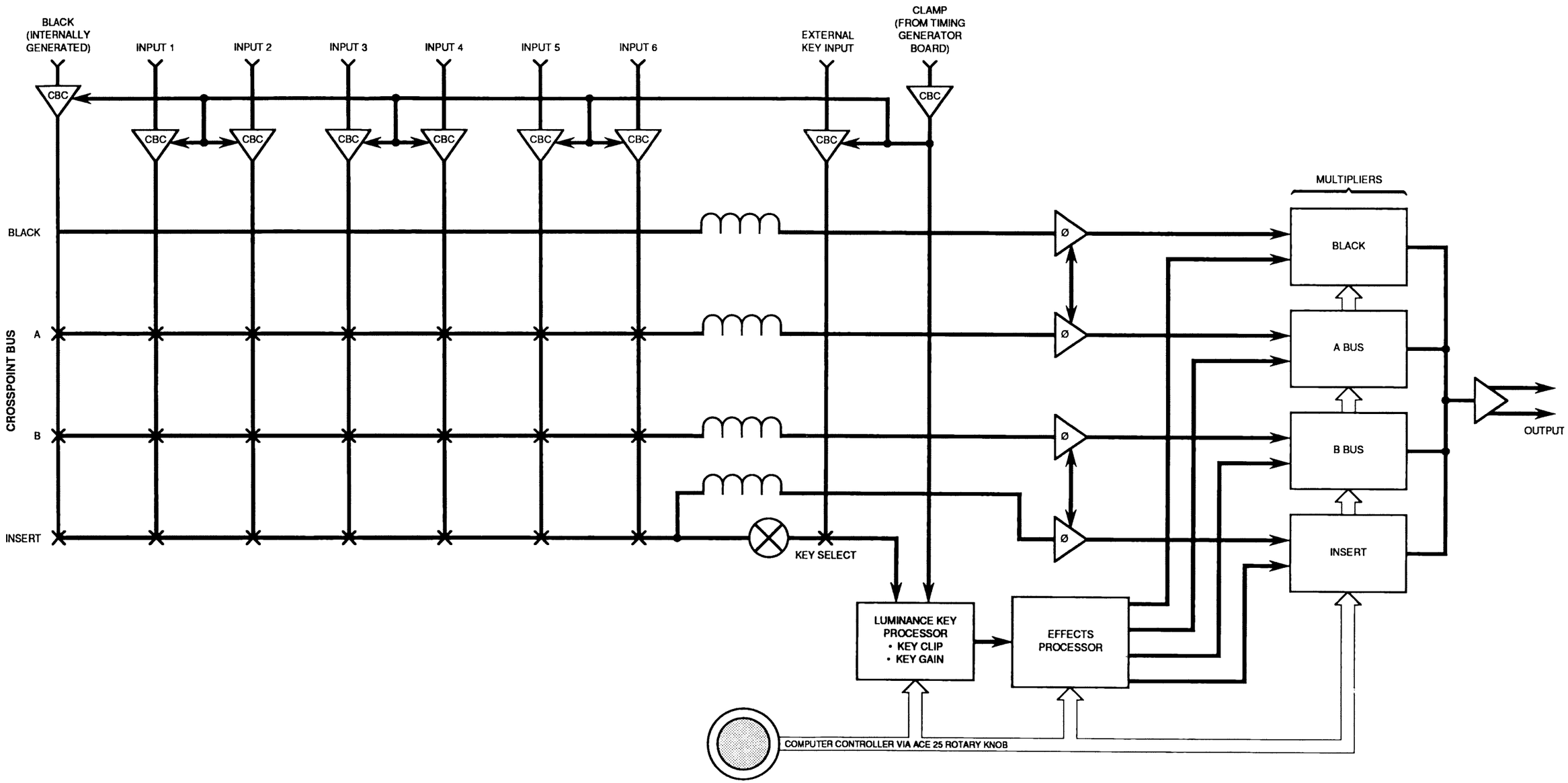


Figure 13-2
Composite Video Switcher Signal Flow Diagram

For the A Bus and B Bus levels of the crosspoint bus, Black video or any of the six video inputs can be selected as the bus output signal. The A Bus and B Bus signals selected by the crosspoints pass through delay stages into phase-shifting clamp-buffer circuits ("ΦSC") before entering the A Bus or B Bus multipliers, respectively.

The Insert Bus signal goes through the crosspoint stage where Black or one of the six input video signals is selected. The Insert Bus output signal is then split into two signals. The top signal path goes through a delay stage into a phase-shifting clamp-buffer ("ΦSC") circuit, before entering the Insert Bus multiplier circuit. The bottom signal path goes to an auto-crosspoint (shown as an "X" within a circle in Figure 13-2). The auto-crosspoint selects Black, one of the six video input signals,the external key input, or a luminance key generated on the switcher. The output signal selected on the lower Insert Bus goes into the Luminance Key Processor.

The Luminance Key Processor generates the luminance key and sets key clip and key gain levels. The Effects Processor block represents the logic used to create the maps for the multipliers to form mixes, fades, keys, and so forth, using control ramp signals. The outputs of the multipliers enter the output amplifier (op-amp), where they are merged to create the final output video signal.

A series of delay jumpers are used to time signals within 10 ns for different signal paths. The phase-shifting clamp-buffer stage ("ΦSC") provides vernier control for fine-tuning timing of the video signals.

13-4 "X" Block Multiplier Circuit

The "X" Block Multiplier Circuit (see Figure 13-3) is used in the four video multipliers, with specific electronic components for each circuit listed in the detail table. The video input "A" comes from the Black "CBC" circuit or the A/B/Insert bus "ΦSC" circuit. Control input "B" comes from the Effects Processor circuit. The outputs "C" and "D" are differential outputs to the output amplifier circuit (op-amp), and "E" is feedback input from the op-amp. This results in a closed loop system which is stable but may be difficult to troubleshoot.

IC "AA" is a linear-to-logrithmic converter which produces very small control voltages that are sent to the pair of differential transistors (UA). The TRAN (transition) adjustment (RA) is used during a mix to match the average dc level between the differential multipliers. The dc, HF and GAIN adjustments affect the signal by changing the feedback input.

13-5 Output Amplifier Circuit

The Output Amplifier Circuit takes the balanced inputs from the multipliers and produces video output signals at 2V peak-to-peak, which leaves a 1 V peak-to-peak signal when terminated at 75Ω. The feedback output goes into the multiplier circuits for high frequency control.

13-6 "CBC" Channel Buffer-Clamp Circuit

The "CBC" circuit (shown in Figure 13-4) is used to buffer and clamp the Black and Input 1 through Input 6 video signals. The clamp signal comes from the Video Timing PWA, as well as the reference video input. Clamping is provided by amplifier UA, which is effectively turned off except when clamp pulse is present during burst interval of composite reference video signal.

13-7 "ΦSC" Phase-Shifting Buffer-Clamp Circuit

Figure 13-5 shows the "ΦSC" circuit which is used for the Black bus, A bus, B bus, and Insert bus. The function of this circuit is to allow limited phase shifting and to clamp the video signal before it enters the multipliers. This circuit has an adjustment (RJ) which shifts the output video phase approximately 10°.

13-8 Dumpster Interface

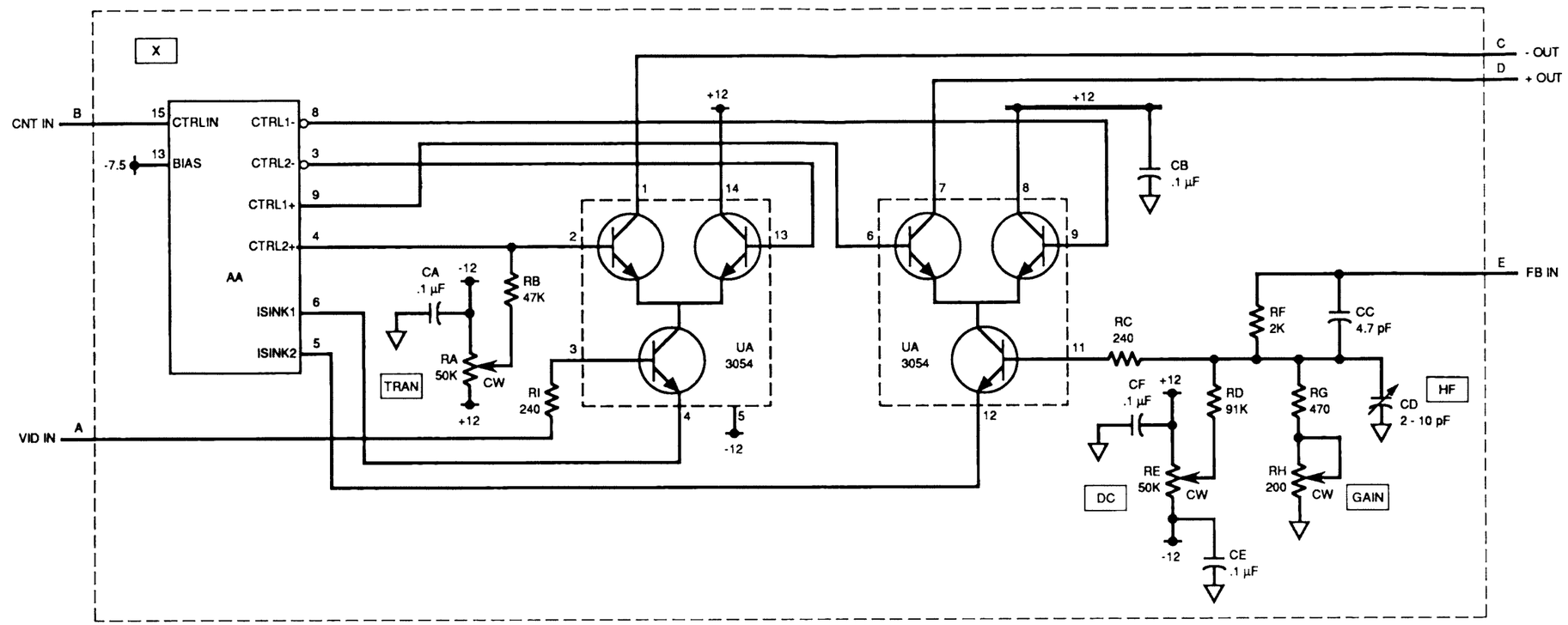
The Dumpster Interface circuitry contains a data latch (U12, U13, U14), decoder (U16, U17, U18), Sample-and-Hold Select section (U27, U28, U32), and a digital-to-analog converter (DAC) (U26). This circuit produces control voltages to control the crosspoint matrix from the DAC. The samples (from the Sample-and-Hold Select section) are used to drive the linear mixers.

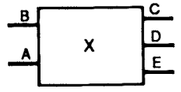
13-9 Linear Mix Adjustments

The linear mix adjustments (R139, R145, R142, R148, R149) compensate for slight differences in analog and/or gate diode drops among the various video signals. These adjustments remove high frequency "breathing" related to transitions. The samples generated from the Dumpster Interface circuitry enable the various linear mix circuits. The outputs from these circuits control the Effects Processor.

13-10 Crosspoint Matrix

The outputs of the "CBC" circuits enter the Crosspoint Matrix where only one crosspoint on a bus can be selected at any given time. The control signals for the matrix are derived from the Dumpster Interface circuit. Jumper J5 selects between NTSC and PAL, with coil L1 providing adjustment as needed. The output signals of the Crosspoint Matrix pass through delays (0 to 150 ns), which are set with jumpers. After the delay stage, these video signals enter the "ΦFC" circuitry.





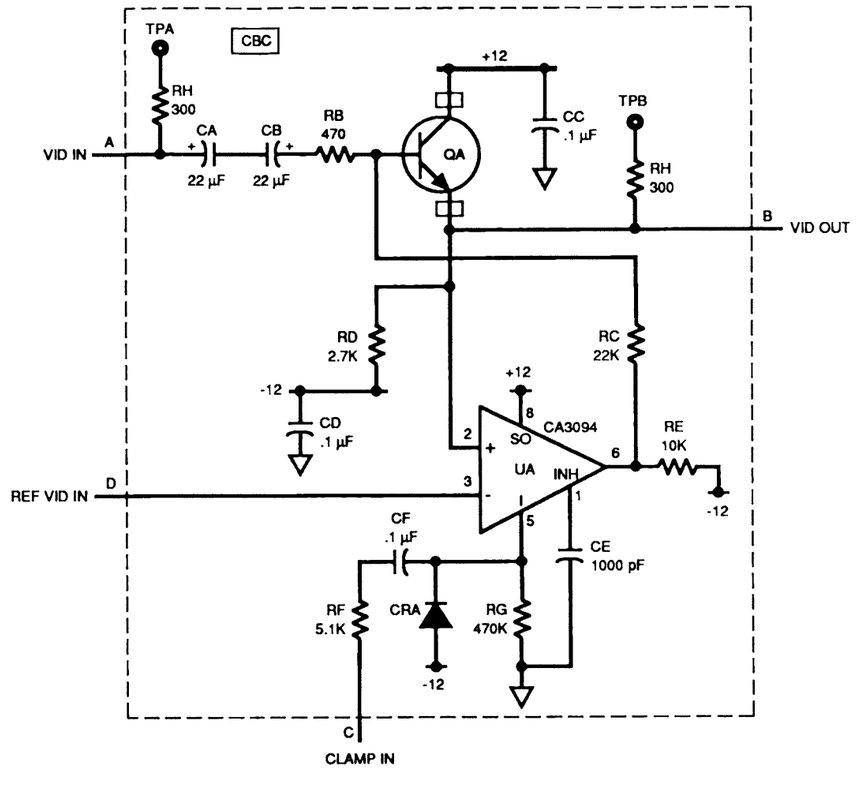
"X" Detail Table

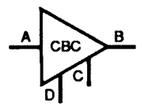
REF DES	AA	UA	RA	RB	RC	RD	RE	RF	RG	RH	RI	CA	CB	CC	CD	CE	CF
X1	34	46	250	249	245	243	242	244	248	247	246	200	197	198	199	202	194
X2	33	45	241	240	237	235	234	236	239	238	212	193	190	191	192	195	185
X3	32	44	233	232	229	227	226	228	231	230	207	185	182	183	184	187	214
X4	35	47	257	259	254	252	251	253	258	256	255	205	210	203	204	206	201

Note

Detail table for general circuit schematic shows actual component designations used for each circuit. Component values (such as ohms) are shown in schematic. Small, simplified diagram, located below schematic, shows the input/output connections for general circuit.

Figure 13-3.
Block Multiplier ("X") Circuit Schematic Diagram





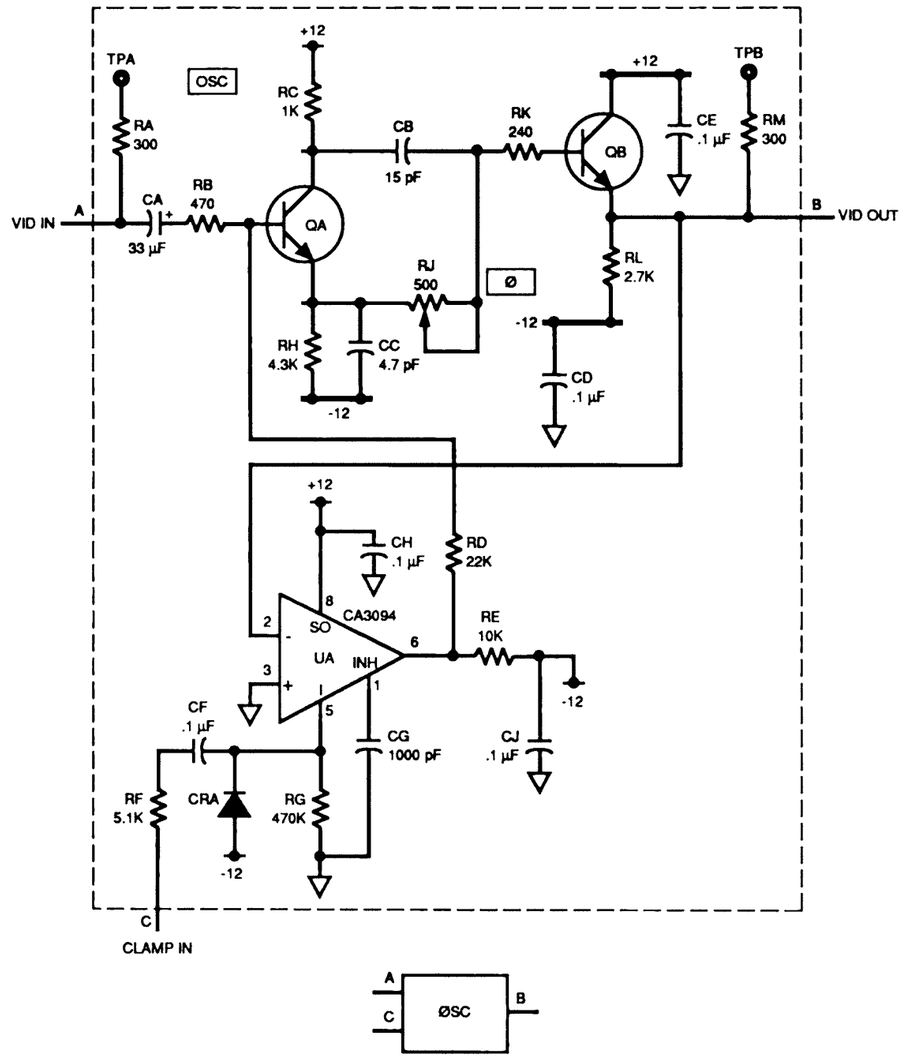
"CBC" Detail Table

REF DES	TPA	TPB	CR	CB	CC	CD	CE	CF	RA	RB	RC	RD	RE	RF	RG	RH	OA	UA	CRA
CBC1	7	8	36	37	38	35	39	41	25	28	31	26	32	34	33	27	3	20	6
CBC2	13	14	56	57	58	55	59	60	53	56	57	54	58	60	59	55	6	23	9
CBC3	11	12	50	51	52	49	53	54	45	48	49	46	50	52	51	47	5	22	8
CBC4	18	19	69	70	71	68	72	73	69	72	73	70	74	76	75	71	8	25	11
CBC5	16	17	63	64	65	62	66	67	61	64	65	62	66	68	67	63	7	24	10
CBC6	20	21	75	76	77	74	78	79	77	80	81	78	82	84	83	79	9	26	12
CBC7	22	23	81	82	83	80	84	85	85	88	89	86	90	92	91	87	10	27	13
CBC8	9	10	43	44	45	42	46	48	35	38	41	36	42	44	43	37	4	21	7

Note

Detail table for general circuit schematic shows actual component designations used for each circuit. Component values (such as ohms) are shown in schematic. Small, simplified diagram, located below schematic, shows the input/output connections for general circuit.

Figure 13-4.
Channel Buffer Clamp ("CBC") Circuit Schematic Diagram



Note

Detail table for general circuit schematic shows actual component designations used for each circuit. Component values (such as ohms) are shown in schematic. Small, simplified diagram, located below schematic, shows the input/output connections for general circuit.

"ØSC" Detail Table

REF DES	CR	CB	CC	CD	CE	CF	CG	CH	CJ	RA	RB	RC	RD	RE	RF	RG	RH	RJ	RK	RL	RM	OR	OB	CRA	UA	TBA	TPB
OSC1	163	167	169	162	166	168	164	165	189	183	184	187	186	210	213	214	188	189	185	182	211	19	18	17	42	44	55
OSC2	157	160	161	155	158	188	156	159	181	174	176	179	178	205	208	209	180	181	177	175	206	17	16	16	41	41	54
OSC3	148	153	154	147	149	152	150	151	213	165	170	169	168	201	203	204	172	173	167	166	202	15	14	15	40	36	37
OSC4	171	175	177	170	172	176	173	174	196	190	192	195	194	215	217	218	196	197	193	191	216	21	20	18	43	50	56

Figure 13-5.
Phase Shifting Clamp ("ΦSC") Circuit Schematic Diagram

13-11 Luminance Key Processor

The Luminance Key Processor forms keys from the external key input (which can only be a luminance key), or from a luminance key generated on the Insert bus. The key level signal (from the sample-and-hold section), is combined with the key video input and clamp signal in a current amplifier. The shifting dc levels determine when the signal goes to zero. The key gain signal from the Dumpster bus goes into a step circuit, which controls the gain of the current amplifier output. A feedback loop prevents over-saturation. U14 selects normal or inverted key type, and is controlled by the key invert signal of the Dumpster bus.

13-12 Effects Processor

The Effects Processor generates the control signals for the four video multipliers. These video multipliers produce the video signal for the output amplifier. The Effects Processor consists of cascaded AND and OR gates which mix the various A, B, Insert, and Key video control signal combinations. The effects key is set up as a downstream keyer over the A bus and B bus. The three control outputs (A, B, and Insert) go into the video multipliers to produce the output video signals. Software ensures that the sum of the A, B, Insert, and Black control signals is unity.

13-13 FUSES, TEST POINTS AND JUMPERS

The following paragraphs describe the fuses, test points and jumpers.

13-14 Fuses

The Composite Video Switcher PWA has one fuse, F1 (P/N 070-443). Fuse F1 is rated at 5.0 amp and soldered on two posts. Refer to Figure 13-1. Replace fuse with equivalent fuse.

13-15 Test Points

Table 13-1 lists the test points and their associated signals.

13-16 Jumpers

Refer to Figure 13-1 for the locations of jumpers on the Composite Video Switcher PWA.

Jumper J5 selects NTSC or PAL operation.

Jumpers J6-J9, J10-J13, J14-J17, and J18-J21 set delay times for video signals. Delay times are measured and set at the factory; these jumpers should not be changed.

Table 13-1. Composite Video Switcher PWA Test Points

Test Point	Signal
TP1	±12V
TP2	+12V
TP3	DGND (Digital Ground)
TP4	DGND (Digital Ground)
TP5	+5V
TP6	DGND (Digital Ground)
TP7	VID6 (Video Input 6)
TP8	VID6C (Video Input 6)
TP9	KEY1
TP10	KEY1C
TP11	VID4 (Video Input 4)
TP12	VID4C (Video Input 4)
TP13	VID5 (Video Input 5)
TP14	VID5C (Video Input 5)
TP15	AGND (Analog Ground)
TP16	VID2 (Video Input 2)
TP17	VID2C (Video Input 2)
TP18	VID3 (Video Input 3)
TP19	VID3C (Video Input 3)
TP20	VID1 (Video Input 1)
TP21	VID1C (Video Input 1)
TP22	BLACK
TP23	BLACKC
TP24	AGND (Analog Ground)
TP25	YB
TP26	YA
TP27	YBLK

(Continued next page)

Table 13-1. Composite Video Switcher PWA Test Points

Test Point	Signal
TP29	KEY VID
TP30	KEY
TP31	K BLNK
TP32	A VID CTRL
TP33	AGND (Analog Ground)
TP34	BLK VID CNTR
TP35	AGND (Analog Ground)
TP36	YI VID
TP37	YI VIDC
TP38	–AR MIX
TP39	–BK MIX
TP40	INS VID CTRL
TP41	YB VID
TP42	–K BLNK
TP43	INS MIX
TP44	YA VID
TP45	B VID CTRL
TP46	BKG KEY
TP47	INS KEY
TP48	B MIX
TP49	A MIX
TP50	Y BLK
TP51	AGND (Analog Ground)
TP52	Y OUT
TP53	NOT USED
TP54	YB VIDC
TP55	YA VIDC
TP56	Y BLK VIDC
TP28	YI

13-17 ADJUSTMENTS

The following paragraphs describe the test equipment and adjustments that are performed on the Composite Video Switcher PWA.

13-18 Test Equipment

Table 13-2 lists the recommended test equipment for performing adjustments on the Composite Video Switcher PWA.

Table 13-2. Recommended Test Equipment

Equipment	Recommended Model
Video Signal Generator	Tektronix 140 or equivalent
Video Signal Generator	Tektronix 147 or equivalent
Video Signal Generator	Tektronix TSG300 or equivalent
Probe, Oscilloscope (2)	Tektronix 6106 or equivalent
Waveform Monitor	Tektronix 1485R or equivalent
Waveform Monitor	Tektronix WFM 300 or equivalent
Color Monitor	Tektronix 655HR or equivalent
Vectorscope	Tektronix 520R or equivalent
Video Distribution System	Dynair 5300 or equivalent
Cable, coax, BNC connector, 75Ω (25 required)	

13-19 Power Supply Checks

Check the following points for the corresponding voltages:

TP1 ±12 V ±0.6V

TP2 +12 V ±0.6V

TP5 + 5 V ±0.25V

13-20 Input Black Timing and Gain

The following procedure is used to set the timing and gain level for the Black Input video signal.

1. Scope Channel 1 to TP22 (Black In) and Channel 2 to TP20 (Y1 In).
2. Adjust the Video Timing PWA H Phase pot (R7) for the leading edge of H sync to be coincident at the 50 points.
3. Scope Channel 1 to TP56 (Y BLK VIDC). Connect scope Channel 2 to TP55 (YA VIDC).
4. Check the leading edge of the H sync signals. The leading edges should be coincident ±5 ns at the 50 points. If the signals are not coincident within specification, change jumpers at DL5 to adjust signal difference to within specification.
5. Connect Channel 1 of oscilloscope to TP20 (VID1). Adjust vectorscope so that the burst vector is on the outer circle, and establish a phase and gain reference point.
6. Connect Channel 1 of oscilloscope to TP22 (BLK IN). Adjust the Timing PWA Burst Phase pot (R10) and the Timing PWA Burst Gain pot (R19) to match the vector phase and gain reference established in the previous step. Adjust burst null to minimize chroma on video portion of signal.
7. Select video black on crosspoint and set wave form monitor to luma only. Adjust burst axis for back porch dc level to equal video dc level.
8. Set wave form monitor to flat. Adjust U and V phase caps on Video Timing PWA for 90° vectors on PAL burst with equal amplitude on both legs.

All these adjustments interact and must be repeated until correct.

13-21 Signal to Noise Adjustments

The following procedure is used to adjust the signal-to-noise levels. A composite video signal is used when checking the video signal. Unit gain is set to match the waveform monitor.

1. Connect Y2 OUT to COMPOSITE VIDEO IN on the test rack.
2. Set the generator to ramp.
3. With the switcher out of the loop, adjust the Distribution Amp to match the video gain to the calibration pulse out of the waveform monitor (cables barreled together).
4. Set the generator to multiburst and make a reference of the waveform monitor (terminated) with the lowest vertical gain setting.
5. Reconnect the cables to the switcher.
6. Connect scope Channel 1 to TP52 (Y OUT) unterminated.
7. Press SHIFT F10 on the comments keyboard to clear switcher functions.
8. Set the generator to ramp.

9. Adjust YA GAIN pot (R247) for unity gain. This is done by matching the calibration pulse to the video ramp ±0.1 IRE.

10. Set the generator to multiburst.

11. Adjust the YA HF cap (C208) for frequency response to be equal to the waveform monitor reference ±1 IRE.

12. Adjust the YA HF cap (C199) to be in the center of its frequency response range.

13. Adjust the YA dc pot (R242) for the back porch to be at 0 Vdc ±2 mV.

14. Push the "+" key and press the shift F1 key until B Bus Level: FF is selected.

15. Set the generator to ramp.

16. Adjust YB GAIN pot (R238) for unity gain. This is done by matching the calibration pulse to the video ramp ± 0.1 IRE.

17. Set the generator to multiburst.

18. Adjust the YB HF cap (C192) for frequency response to be equal to the waveform monitor reference ±1 IRE.

19. Adjust the YB dc pot (R234) for the back porch to be at 0 Vdc ±2 mV.

20. Set the generator to ramp.

21. Press F9, then, F4 until KEY CLIP: 00 is selected.

22. Adjust YI GAIN pot (R230) for unity gain, by matching the calibration pulse to the video ramp ±0.1 IRE.

23. Set the generator to multiburst.

24. Adjust the Y1 HF cap (C184) for frequency response to be equal to the waveform monitor reference 1 IRE.

25. Adjust the YI dc pot (R226) for the back porch to be at 0 Vdc ±2 mV.

26. Set the generator to ramp and the chroma vector to the outer vectorscope circle and establish a phase reference point. This will be used to measure transition shift.

Note

At this point, refer to paragraph 13-23, and perform preliminary phase pot adjustments. Composite Video Switcher PWA must be close to specifications to see phase shift during transitions.

13-22 Transition (Linear Mix) Adjustments

The following procedures are used to set the timing for the video signals used in the transition combinations.

To adjust the A Bus to B Bus transitions:

1. Attach scope to R239-1.
2. Preset R250 (YA TRAN) for 0V. This may need to be readjusted later.
3. Press SHIFT F10 then SHIFT F5.
4. Adjust the B MIX LIN pot (R139) for minimum phase shift on the vectorscope during the transition. Phase shift should be less than ±0.75°. Frequency response dip during the transition should be less than ±1 IRE.
5. Adjust YB TRANS pot (R241) for dc disturbance to be less than ±10 mV (unterminated) measured at the back porch.

To adjust the A Bus to INSERT Bus transitions:

1. Press SHIFT F10, then CTRL F1.
2. Adjust the INS MIX LIN pot (R145) and AK MIX LIN pot (R148) for minimum phase shift on the vectorscope during the transition. Phase shift should be less than ± 0.75°. Frequency response dip during the transition should be less than ±1 IRE.
3. Adjust YI TRANS pot (R233) for dc disturbance to be less than ±1 IRE.
4. The Insert switching glitches on the front and back porch should be less than ±20 mV (unterminated).

To adjust the A Bus to BLACK Bus transitions:

1. Press SHIFT F10.
2. Press F1 until A Bus Crosspoint: FE is selected.
3. Press F2 until B Bus Crosspoint: FE is selected.
4. Press SHIFT F7.
5. Adjust Y BLK dc pot (R251) for the back porch to be at 0 Vdc ±2 mVdc.
6. Adjust BLK FADE LIN pot (R142) for minimum phase shift on the vectorscope during the transition. Phase shift should be less than ±0.75°.
7. Adjust Y BLK TRAN pot (R257) for minimum dc transition disturbances. dc disturbances should be less than ±10 mVdc (unterminated).
8. Adjust Y BLK GAIN pot (R256) for the black amplitudes to be the same (±5 mV). The black gains are adjusted by matching the setup signal levels.

9. Adjust Y BLK HF (C204) for the black burst vector to be equal to the YA burst vector.

To adjust the B Bus to BLACK Bus transitions:

Note
Use Composite Black Burst to set up BLK FADE LIN pot and Black Frequency Response in this procedure.

1. Press the space bar on the keyboard.
2. Press SHIFT F8.
3. Verify the dc transition disturbances are less than ±10 mVdc (unterminated), and phase shift is less than ±0.75°. If they are not, adjust the Y BLK TRAN pot (R257) and the BLK FADE LIN pot (R142). If either of these adjustments is made, the A Bus to BLACK Bus transitions must be rechecked.

To adjust the B Bus to INSERT Bus transitions:

1. Press SHIFT F10, then CTRL F2.
2. Adjust the BLK MIX LIN pot (R149) for minimum phase shift during transition. Phase shift should be less than ±0.75°. Frequency response dip during transition should be less than ±1 IRE. A slight adjustment of the INS MIX LIN pot (R145) may be necessary. If so, recheck the A to INSERT Transitions.
3. Verify the dc transition disturbances are less than ±10 mVdc (unterminated). If they are not, split the errors with the A to INSERT Transitions. If they are still out, adjust the YA TRANS pot (R250) and YB TRANS pot (R241) and redo the Y CHANNEL Transition Adjustments.
4. The insert switching signal disturbances on the front and back porch should be less than ± 20 mV (unterminated).

To adjust the Chroma Trap Null timing:

1. Attach oscilloscope to TP 29 (KEY VID). Ramp in oscilloscope. Scope BW to 20 MHz.
2. Adjust L1 to null chroma at TP29 to less than 20 mV peak-to-peak.
3. Check that spikes at start and end of burst area are less than 80 mV peak-to-peak.

To adjust the Key Clip timing:

Note

Add sweep signal test here to observe wave shape as key gain is varied. Gain bandwidth product causes rolloff of response as gain increases. Normal response is slight dip, then peak, then rolloff.

1. Connect scope probe to TP30.
2. Press SHIFT F10, then press F9.
3. Press F10 until Key Bus Crosspoint: FB is selected (color bars).
4. Press "+" for Turbo mode.
5. Press F5 to set Key Gain: 00.
6. Press F3 and F4 to set the Key Clip from 00 to FF. With the Key Clip at 00, the key signal at TP30 should be +0.3 V ±0.1 V.
7. With the Key Clip at FF, the key signal at TP30 should be -2.8 V ±0.1 V.
8. Press "-" to turn Turbo mode off.
9. Connect the scope probe to TP52 (Y OUT), and set the vertical gain to maximum.
10. By pressing Key Clip (F3 and F4), verify that there are seven counts of dead zone (00-07) at the low end and seven counts of dead zone at the high end (F8-FF). The clip runs from 0EH to F4H on the Component Switcher PWA.
11. Connect the scope probe to TP47 (INS KEY). Check the dc for Key Clip at 00 and at FF. With the Key Clip at 00, the dc level should be at least +2.3 V. With the Key Clip at FF, the dc level should be at least -0.2 V.

13-23 Timing

The following adjustment for Y Channel timing is done with a composite 2T signal keyed over the composite white signal from the 147 Video Signal Generator:

1. Set the program control switch to AUXILIARY and the REMOTE/LOCAL switch to LOCAL.
2. Set the AUXILIARY PEDESTAL for the white level to be 100 IRE.

To adjust the Insert video signal timing:

Note

This adjustment sets reference phase for ACE 25 system.

1. Set the color monitor to NTSC.
2. Set the 147 Video Signal Generator to 2T signal.

3. Press SHIFT F10.
4. Set the A Bus Crosspoint: F7 (white video) with F1.
5. Set the B Bus Crosspoint: F7 (white video) with F2.
6. Set the KEY Bus Crosspoint: FD (2T video) with F10.
7. Press F9 to initialize key.
8. Press F7 to select Y Bus Key.
9. Set KEY Gain: 04 with F5 and F6.
10. Press "+" to select the Turbo mode.
11. Set KEY Clip: 2C with F3 and F4.
12. Press the "-" to leave the Turbo mode.
13. Fine tune the KEY Clip, using the X20 horizontal mag on the waveform monitor.
14. While looking at the picture monitor, adjust the YI phase shifter (R173) for the 2T pulse to be visually centered in the key hole. If the 2T pulse can not be centered in the key hole, reset the jumpers for the YI delay line (DL 2). If the delay line jumpers are reset, all of the Y Channel adjustments must be redone.
15. Make sure the Composite 2T signal is connected to the External Key input. Press F7 (Key Source Select) and verify that the 2T video is present in EXTERNAL and Y Bus.
16. Toggle between Y BUS and EXTERNAL and compromise the setting of R490. The composite switcher PWA does not have Chroma Key capability.

To adjust the YA video signal timing:

1. Set the 147 Video Signal Generator for composite ramp.
2. Set the vectorscope Phase Reference to EXT.
3. Press Shift F10 and F9.
4. Press "+" to select the Turbo mode.
5. Set the Key Clip Level: 00 with F4.
6. Set the reference phase signal for YI on the vectorscope within the calibration circle.
7. Press Shift F10 (A Bus Selected).
8. Adjust YA PHASE pot (R189) for the signal to match the phase reference.

Note

If phase pot can not be adjusted to match reference, YA delay line (DL 4) jumpers must be reset. If delay line jumpers are reset, all Y Channel adjustments must be redone.

To adjust the YB video signal timing:

1. Select the B Bus by pressing SHIFT F1 until B Bus Level: FF is reached.

2. Adjust YB PHASE pot (R181) for the signal on the vectorscope to match the reference phase.

Note

If phase pot can not be adjusted to match reference, YB delay line (DL 3) jumpers must be reset. If delay line jumpers are reset, all Y Channel adjustments must be redone.

To adjust the Black video signal timing:

1. Select the A to BLK transitions by pressing SHIFT F7.

2. Adjust Y BLK PHASE pot (R197) for the signal on the vectorscope to match the reference phase.

Note

If phase pot can not be adjusted to match reference, Y BLK delay line (DL 5) jumpers must be reset. If delay line jumpers are reset, all Y Channel adjustments must be redone.

13-24 Differential Phase and Gain

Differential phase and gain for all crosspoints should be less than 0.7% (0.7 degrees), measured at 10, 50, and 90% , APL (Amplitude Peak Level), using a Tektronix 1410 Generator.

13-25 Path Length Accuracy

Establish a phase reference on the YA bus using Y1 in. For all crosspoints, phase shift should be less than 1° .

13-26 Crossfade Luminance and Chrominance Linearity

The Luminance Linearity should have less than 0.5 gain at the 10 mVdc level. The Chrominance Linearity should have less than 1.5 gain, and be within 1.5° phase. (Phase was checked as mix linearity pots were set.)

13-27 Crosstalk

The crosstalk measurement should be greater than 55 dB at subcarrier.

13-28 K Factor

The K pulse should be less than 0.5. The K pulse-to-bar measurement should be less than 0.5.

SECTION 14

COMPONENT VIDEO SWITCHER PWA

14-1 INTRODUCTION

The Component Video Switcher PWA (P/N 1445928) is an internal video switcher for component analog video signals. This PWA plugs into the Switcher Backplane PWA, with four 64-pin connectors providing power and signal connections. External input and output connections are located on the lower rear panel of the Edit Controller unit. An extension board is available for test and adjustment procedures. Figure 14-1 shows the Component Video Switcher PWA and identifies fuses, jumpers and adjustment points.

14-2 THEORY OF OPERATION

The following paragraphs describe theory of operation for the Component Video Switcher PWA and its primary circuits. Figure 14-2 is a diagram showing the main video signal paths for the Y channel on the Component Video Switcher PWA. The Composite Video Switcher PWA processes three video signal channels: Y, Pr, and Pb. Y is the luminance signal, and Pr and Pb are the color difference signals. The Pb and Pr (color difference) channels are similar to the Y channel, with differences noted.

14-3 General Description

The Black video signal is internally generated on the Video Timing PWA from the referene video signal supplied to the ACE 25. Six external video signal inputs (Input 1 through Input 6) for the three channels (Y, Pr, and Pb) enter the switcher through the Switcher Backplane PWA from the BNC connectors mounted on the Edit Controller rear panel. The external key video signal input comes to the switcher in the same manner. A clamp signal from the Video Timing Generator PWA is used by the switcher to process the video signals.

The Black input passes through a buffering circuit (shown as a triangle labeled "YBC" in Figure 14-2). The six external inputs for the Y channel pass through "YBC" buffering circuits. The six external inputs for the Pr and Pb channels pass through "CBC" clamping and buffering circuits. The external key input is used with the Y channel only, and passes through a "CBC" circuit. The primary difference between the "YBC" and "CBC" circuits is the use of the clamp signal for the "CBC" circuit. The Y channel inputs are clamped from sync tip, which may not be present in the Pr and Pb signals.

The Black input and six external inputs (for each channel) pass through the clamping and buffering stages to the crosspoint buss stage, which has four levels: Black Bus, A Bus, B Bus, and Insert Bus. The Black level is not a complete crosspoint bus, because it only has the Black video signal. This Black level passes through a delay stage into a clamp-buffer circuit ("CBC") before entering the Black multiplier circuit.

For the A Bus and B Bus levels of the crosspoint bus, Black video or any of the six video inputs can be selected as the bus output signal. The A Bus and B Bus signals selected by the crosspoints pass through delay stages into phase-shifting clamp-buffer circuits ("ΦSC") before entering the A Bus or B Bus multipliers, respectively.

The Insert Bus signal goes through the crosspoint stage where Black or one of the six video signals is selected. The Insert Bus output signal is then split into two signals. The top signal path goes through a delay stage into a phase-shifting clamp-buffer ("ΦSC") circuit, before entering the Insert Bus multiplier circuit. The bottom signal path goes to an auto-crosspoint (shown as an "X" within a circle in Figure 14-2). This auto-crosspoint is only present for the Y channel. The auto-crosspoint selects Black or one of the six video input signals. If the auto-crosspoint is closed, a chroma key can be selected at a later crosspoint. If the auto-crosspoint is open, the external key input can be used to cut a key (shown by the crosspoint labeled "KEY SELECT" in Figure 14-2). The lower Insert Bus video signal continues through a delay stage to a crosspoint, which is linked to the Chroma Key Processor. This crosspoint selects the video signal entering the Luminance Key Processor.

The Chroma Key Processor and Hue Adjust circuit has video signal inputs from the Pb Bus and Pr Bus. The processor generates a key signal based on color information. This key signal is converted to a luminance signal. The rotary knob on the ACE 25 keyboard is used to adjust hue.

The Luminance Key Processor generates the actual key video signal, using either the signal from the Chroma Key Processor, or a true luminance signal from the Insert Bus. The rotary knob on the ACE 25 keyboard adjusts the key clip level and the key gain level. The output signal from the Luminance Key Processor goes to the Effects Processor.

The Effects Processor contains the logic circuitry used to create the maps for the Black, A Bus, B Bus and Insert Bus multipliers to form mixes, fades, keys, and other effects. The output of the four multipliers enters a multiplier op-amp, which creates the final video signal output.

A series of delay jumpers is used to time signals within 10 ns for the different channels and signal paths. Fine adjustment of timing is done in the phase-shifting clamp-buffer ("ΦSC") stages.

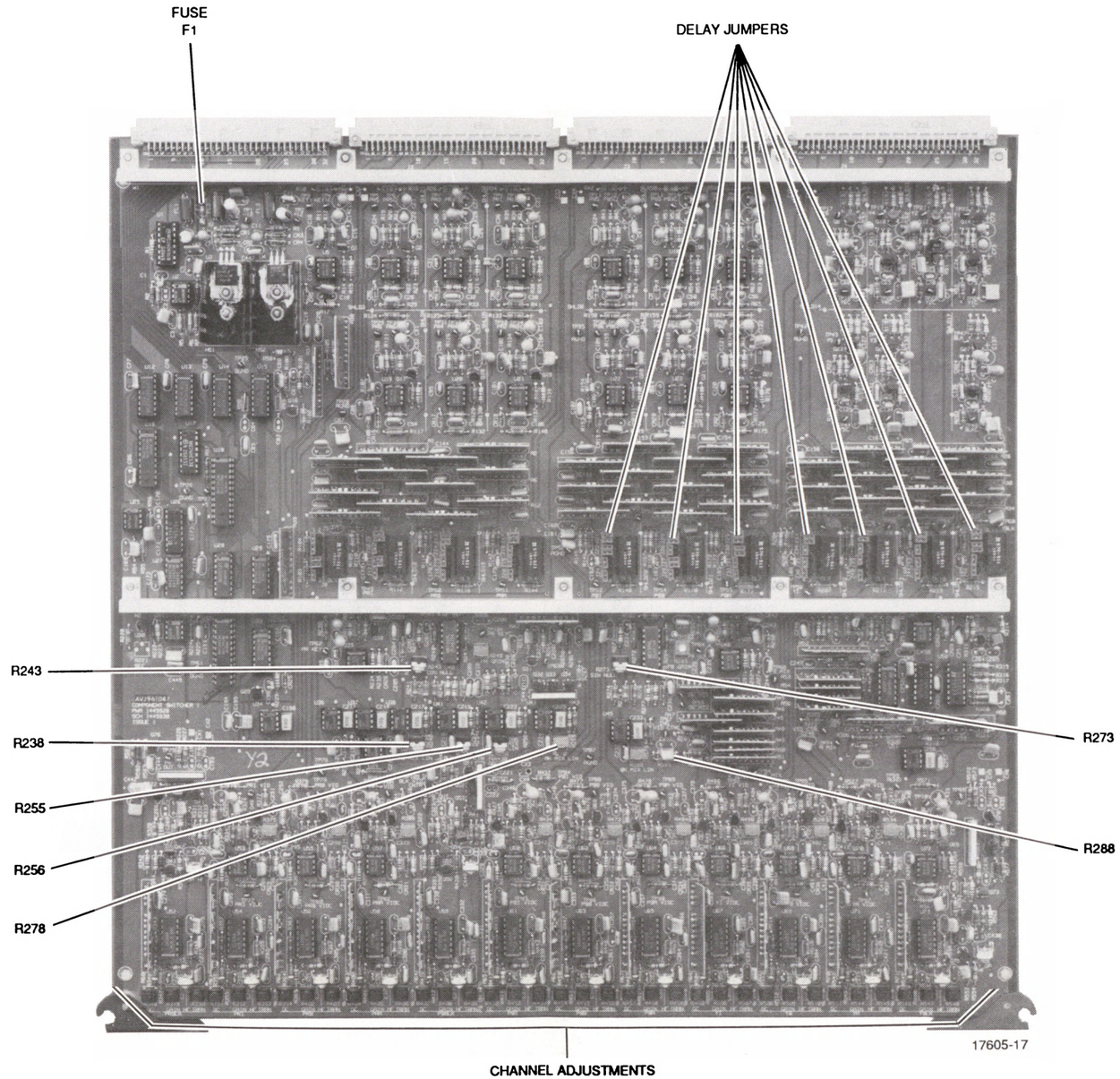


Figure 14-1.
Component Video Switcher PWA

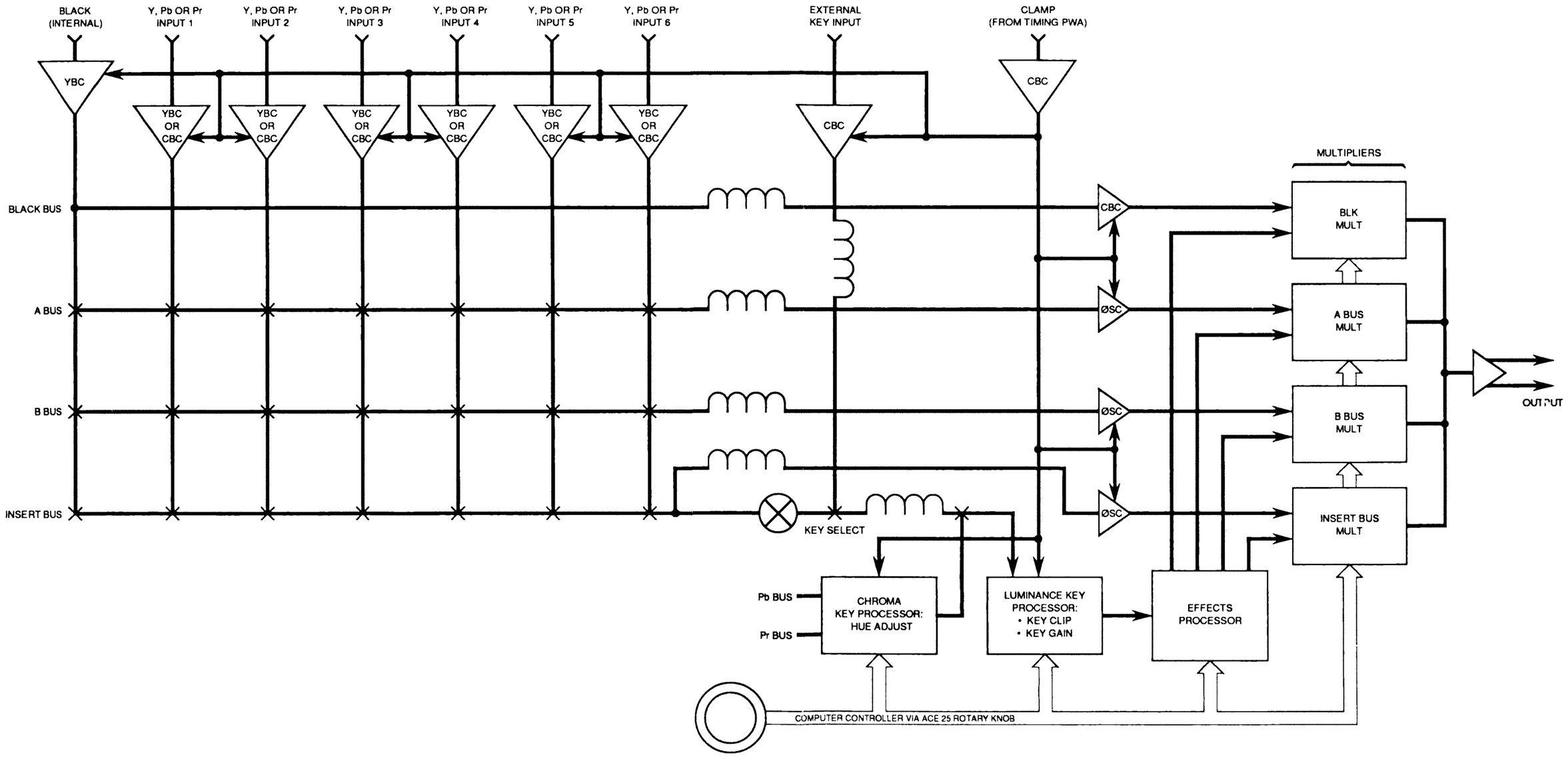


Figure 14-2.
Component Video Switcher Signal Flow Diagram

14-4 Block Multiplier ("X") Circuit

The Block Multiplier ("X") circuit (see Figure 14-3) is used 12 times on the board, with specific electronic components listed for each circuit in the detail table. The video input "A" comes from the Black Channel Buffer-Clamp ("CBC") circuit or the A/B/Insert bus Phase-Shifting Clamp-buffer ("ΦSC") circuit. Control input "B" comes from the Effects Processor circuit. The outputs "C" and "D" are differential outputs to the Multiplier Output Amplifier ("XOA") circuit, and "E" is feedback input from the "XOA" circuit. This results in a closed loop system which is stable but may be difficult to troubleshoot.

IC "AA" is a linear-to-logrithmic converter which produces very small control voltages that are sent to a pair of differential transistors (UA). The TRAN (transition) adjustment (RA) is used during a mix to match the average dc level between the differential multipliers. The dc, HF, and GAIN adjustments affect the signal by changing the feedback input.

14-5 Luminance Buffer/Clamp ("YBC") Circuit

The Luminance Buffer-Clamp ("YBC") circuit (shown in Figure 14-4), does two things: (1) it performs an impedance transformation from high to low; and (2) it clamps the sync tip to ground (0V). Two emitter-follower stages are incorporated in the circuit, with a diode clamp in the middle. This circuit is used for the Y inputs (Black, Y1-Y6) shown in the top portion of Figure 14-2. Outputs from this circuit go into the crosspoint bus stage.

14-6 Multiplier Output Amplifier ("XOA") Circuit

The Multiplier Output Amplifier ("XOA") circuit (shown in Figure 14-5) takes the balanced inputs from the multipliers and produces output signals at 2V peak-to-peak. This signal becomes a 1V peak-to-peak signal when terminated at 75Ω. The feedback output goes to the multipliers for high frequency control.

14-7 Channel Buffer-Clamp ("CBC") Circuit

The Channel Buffer-Clamp ("CBC") circuit (shown in Figure 14-6) is used in the two color difference channels (Pb and Pr) to buffer and clamp video signal inputs. The clamp signal comes from the Video Timing PWA, as well as the reference video input. Clamping is provided by amplifier UA, which is effectively turned off except when clamp pulse is present during burst interval of composite reference video signal.

14-8 Phase-Shifting Clamp ("ΦSC") Circuit

The Phase-Shifting Clamp ("ΦSC") circuit is shown in Figure 14-7. This circuit is used for the A bus, B bus, and Insert bus for all three channels (Y, Pb, and Pr). The "ΦSC" circuit allows limited phase shifting and clamps the video signal before it enters the multipliers. This circuit has an adjustment (RJ) which shifts the output video phase approximately 10 degrees.

14-9 Dumpster Interface

This section of circuitry (U12, U13, U14, U16, U17, U18, U25, U26, U27, U28, and U32) contains the digital logic that turns signals from the Dumpster bus into direct control signals for the switcher.

14-10 Linear Mix Adjustments

The linear mix adjustments compensate for slight differences in analog and/or gate diode drops among the various video signals. These adjustments remove high frequency "breathing" related to transitions. The sample-and-hold control signals from the Dumpster Interface circuitry activate the various linear mix circuits.

14-11 Y Crosspoint Matrix

The output of the "YBC" circuits (for the Y channel) enter the Y crosspoint matrix, where only one crosspoint on a bus can be selected at any given time. The control signals come from the Dumpster Interface circuitry. Jumper J49 is set to the SCB position (Sync/Composite Blanking) for video standards which need sync on the color difference channels. The Y BLK signal is used as the color difference BLK input. The dc position is used for non-sync video standards. The output signals of the Y crosspoint matrix pass through delays (0 to 150 ns) which are set with jumpers (typically at 140 ns). After the delay stage, these video signals enter the ΦSC circuitry.

14-12 Color Difference Channel Crosspoint Matrix

The Pb and Pr color difference channels each have a crosspoint matrix and delay stages similar to the Y channel. The output signals from the matrix for each channel are fed into the Phase-Shifting Clamp ("ΦSC") circuitry.

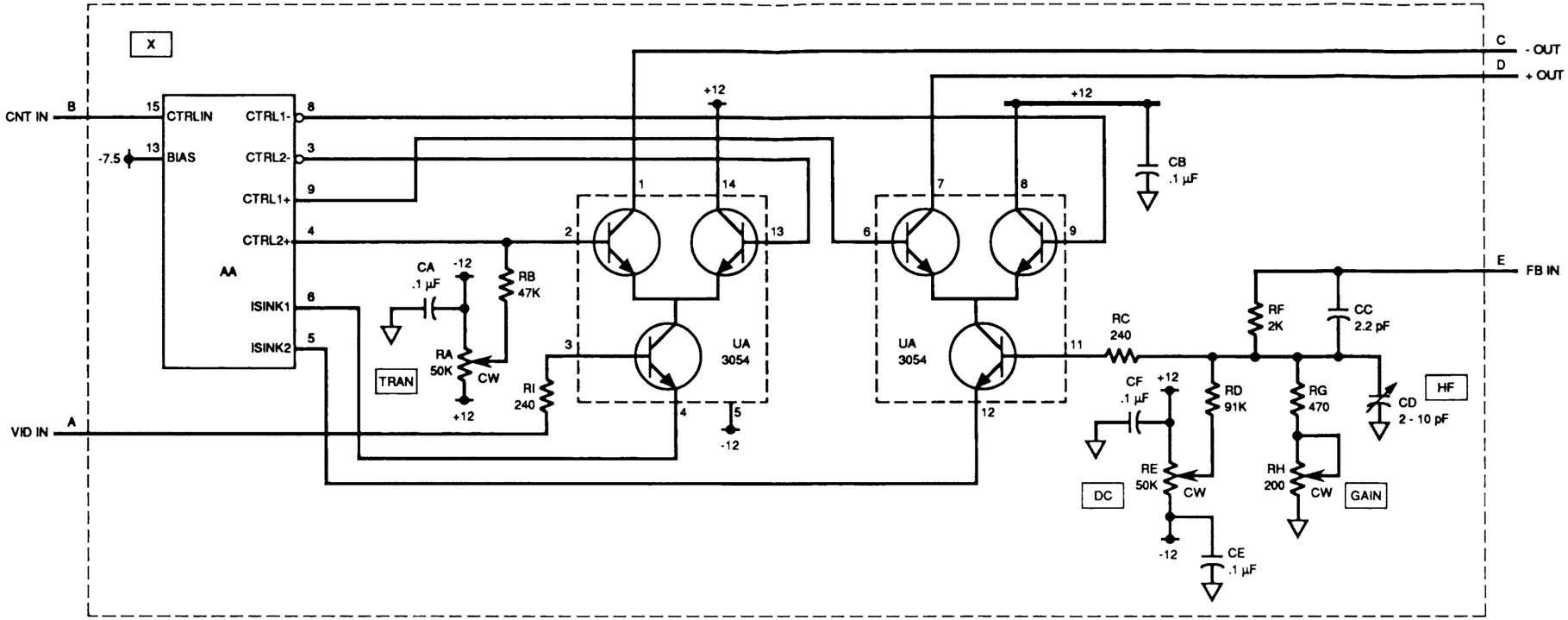
14-13 Chroma Key Processor

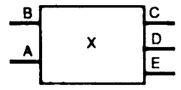
The Chroma Key Processor circuitry develops a chroma key signal using the Pb and Pr input signals. It has two multipliers (U40 and U44) for the COSINE and SIN functions. Pb gain and Pr gain can be adjusted to match the chroma key signal. Discrete comparators Q32/Q33/Q34 produce a positive chroma key signal, with all other colors negative. Two crosspoints are incorporated into this circuit. One selects the EXT key or Y BUS key signal, while the other selects the key fill video. A set of delay jumpers allows timing adjustments to be made if necessary.

14-14 Luminance Key Processor

The Luminance Key Processor forms keys from three sources: (1) the output of the Chrominance Key Processor, which is treated as a luminance signal; (2) the external key source, which can only be a luminance key; and (3) the luminance key generated on the Insert bus.

The key level signal (from the sample-and-hold section of the Dumpster Interface circuitry), is combined with the key video input and clamp signal in a current amplifier (U47, A52). The shifting dc levels determine when the signal goes to zero. The key gain signal from the Dumpster bus goes into a step circuit (U49, U50), which controls the gain of the current amplifier output. Q37/Q38 form a feedback loop to prevent over-saturation. U48 selects normal or inverted key type, and is controlled by the key invert signal of the Dumpster bus.





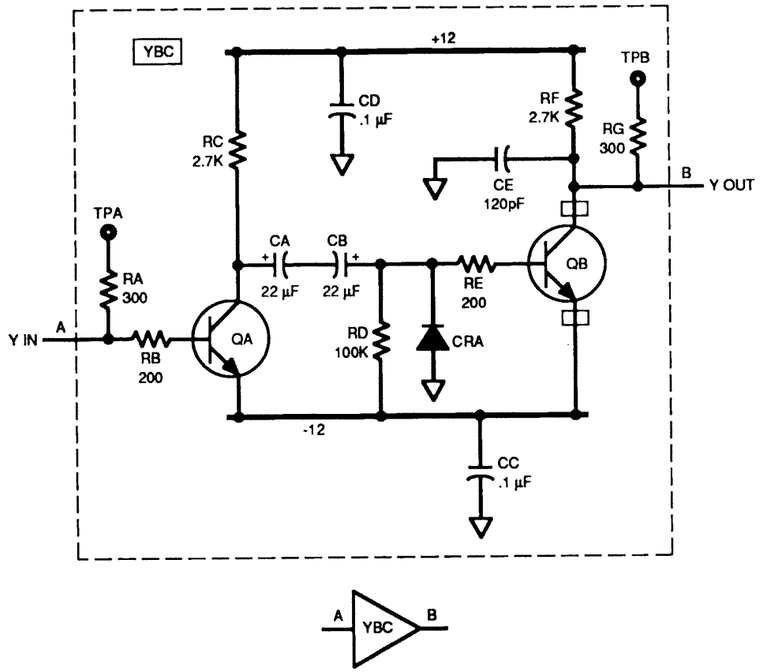
"X" Detail Table

REF DES	AA	UA	RA	RB	RC	RD	RE	RF	RG	RH	RJ	CA	CB	CC	CD	CE	CF
X1	70	71	545	539	540	542	511	543	541	544	612	421	418	419	420	453	396
X2	69	69	510	516	514	513	508	512	515	509	611	394	397	392	393	395	387
X3	68	67	507	502	500	504	460	505	583	506	610	391	383	389	390	388	366
X4	71	73	548	555	551	549	546	550	552	547	609	424	426	422	423	425	417
X5	67	65	459	465	464	462	457	461	463	458	608	364	357	362	363	365	454
X6	66	63	456	448	447	450	454	451	449	455	607	361	353	359	360	358	340
X7	65	61	453	443	413	412	410	411	444	452	606	338	341	336	337	339	331
X8	64	59	409	415	419	418	407	417	416	408	605	335	330	333	334	332	310
X9	63	58	406	398	397	400	404	401	399	405	604	308	311	306	307	309	300
X10	62	56	403	367	363	364	354	365	366	402	603	303	301	303	304	302	284
X11	61	54	353	359	357	356	351	355	358	352	602	282	285	200	281	283	275
X12	60	52	350	344	343	346	348	347	345	349	601	277	274	278	279	276	None

Note

Detail table for general circuit schematic shows actual component designations used for each circuit. Component values (such as ohms) are shown in schematic. Small, simplified diagram, located below schematic, shows the input/output connections for general circuit.

Figure 14-3.
Block Multiplier (X) Circuit Schematic Diagram



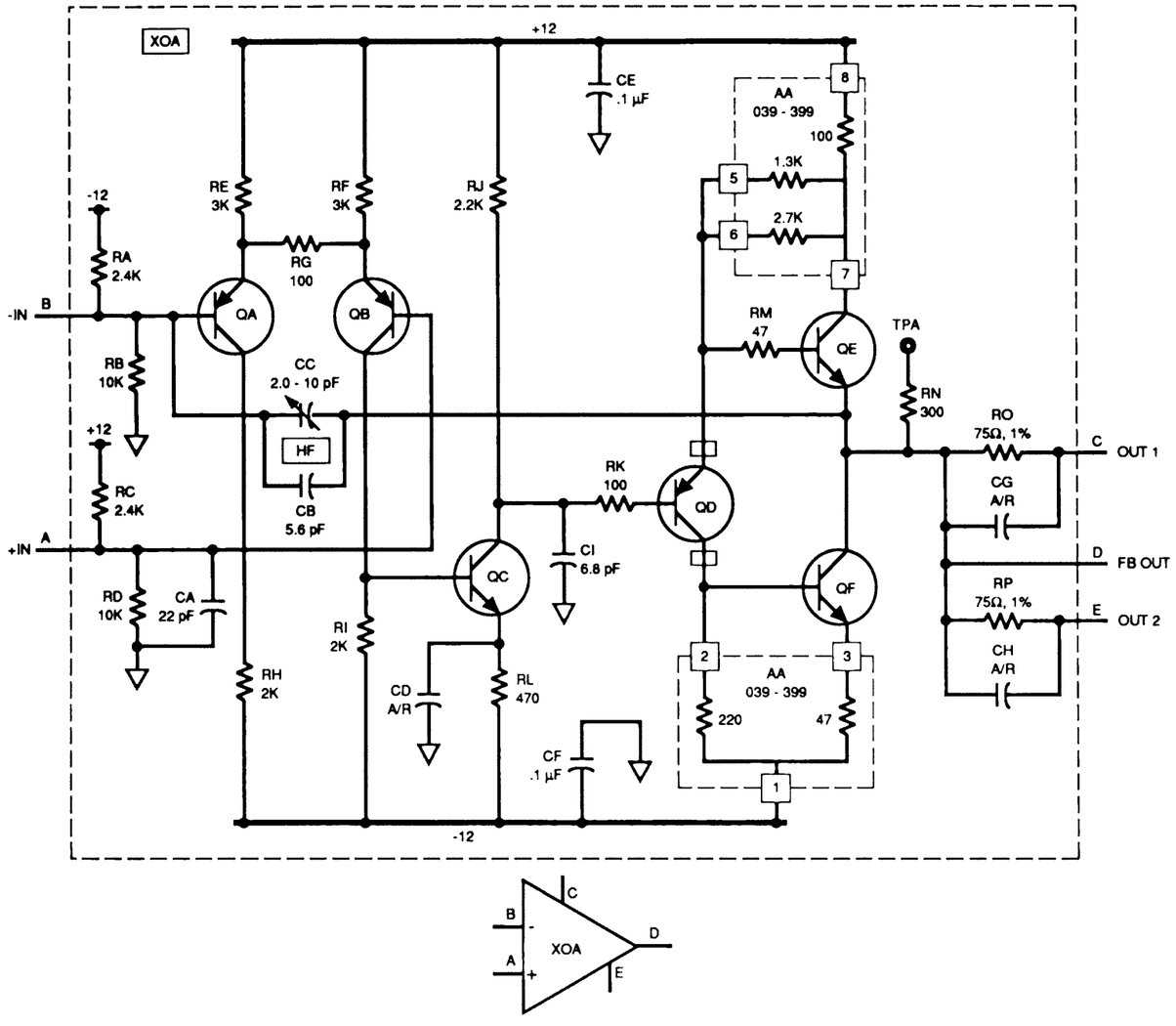
Note

Detail table for general circuit schematic shows actual component designations used for each circuit. Component values (such as ohms) are shown in schematic. Small, simplified diagram, located below schematic, shows the input/output connections for general circuit.

"YBC" Detail Table

REF DES	CR	CB	CC	CD	CE	RA	RB	RC	RD	RE	RF	RG	CR	CB	CRA	TPA	TPB
YBC1	137	138	136	140	139	197	198	199	200	201	202	203	27	28	24	47	48
YBC2	72	73	74	76	75	75	76	77	85	84	93	92	14	15	15	23	24
YBC3	67	68	69	71	70	72	73	74	83	82	91	90	12	13	14	21	22
YBC4	132	133	131	135	134	194	195	196	192	193	191	190	25	26	23	45	46
YBC5	62	63	64	66	65	69	70	71	81	80	89	88	10	11	13	19	20
YBC6	127	128	126	130	129	183	184	185	187	186	189	188	23	24	22	43	44
YBC7	57	58	59	61	60	66	67	68	79	78	87	86	8	9	12	17	18

Figure 14-4.
Luminance Buffer/Clamp ("YBC") Circuit Schematic Diagram



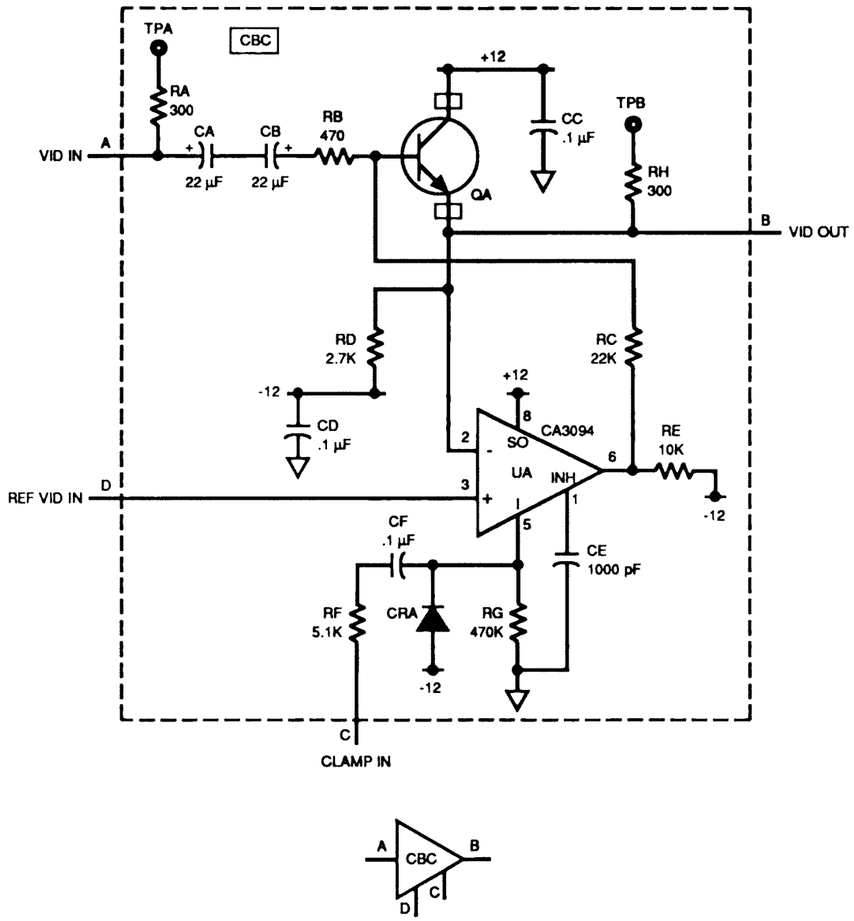
Note

Detail table for general circuit schematic shows actual component designations used for each circuit. Component values (such as ohms) are shown in schematic. Small, simplified diagram, located below schematic, shows the input/output connections for general circuit.

"XOA" Detail Table

REF DES	RA	RB	RC	RD	RE	RF	RG	RH	RI	RJ	RK	RL	RM	RN	RO	RP	CA	CB	CC	CD	CE	CF	CG	CH	CI	OA	OB	OC	OD	OE	OF	AA	TPA
XOA1	561	562	558	559	554	557	556	553	560	577	576	563	575	572	574	573	428	438	439	436	446	437	435	434	462	75	74	73	72	71	70	59	107
XOA2	425	426	390	389	391	392	595	420	421	424	423	422	429	428	430	431	325	326	440	323	445	324	221	222	463	56	55	54	52	51	53	41	83
XOA3	332	333	328	329	341	342	340	339	338	331	326	327	322	226	227	228	268	269	273	266	444	267	192	193	464	44	43	42	40	39	41	40	75

Figure 14-5.
Multiplier Output Amplifier ("XOA") Circuit Schematic Diagram



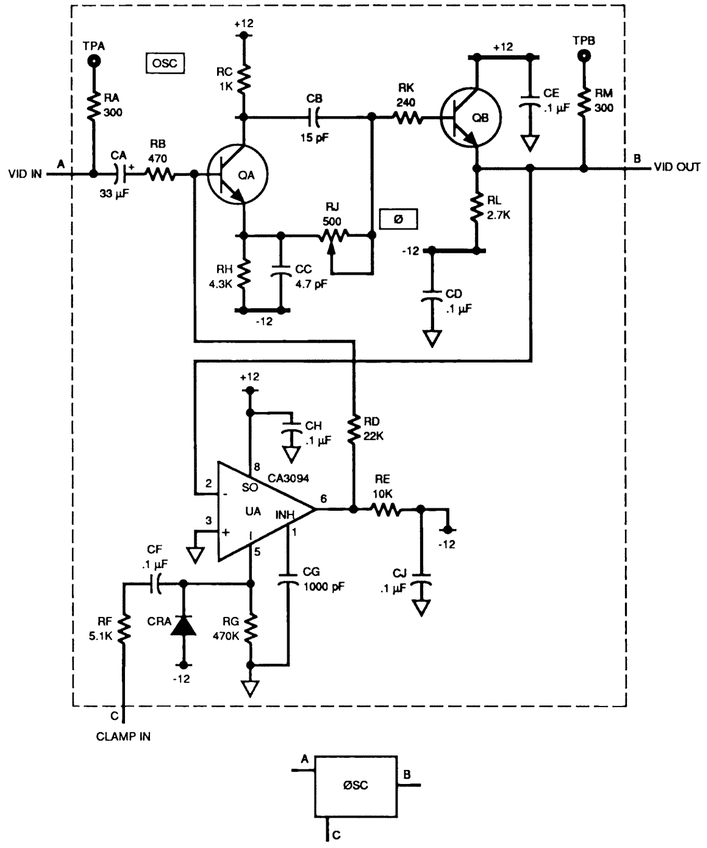
Note

Detail table for general circuit schematic shows actual component designations used for each circuit. Component values (such as ohms) are shown in schematic. Small, simplified diagram, located below schematic, shows the input/output connections for general circuit.

"CBC" Detail Table

REF DES	TPA	TPB	CR	CB	CC	CD	CE	CF	RA	RB	RC	RD	RE	RF	RG	RH	OA	UA	CRA
CBC1	3	4	13	14	15	16	17	18	10	13	14	11	15	17	16	12	1	5	5
CBC2	64	103	241	240	242	243	239	244	296	287	298	289	291	290	292	583	35	46	27
CBC3	62	104	200	201	203	204	202	205	230	231	232	233	234	244	235	594	30	35	26
CBC4	100	101	433	432	431	430	429	427	571	570	565	568	564	567	566	569	69	72	
CBC5	15	16	51	52	53	54	55	56	58	61	62	59	63	65	64	60	7	11	11
CBC6	40	41	122	123	124	121	120	125	162	181	177	179	178	175	176	180	22	24	21
CBC7	13	14	45	46	47	48	49	50	50	53	54	51	55	57	56	52	6	10	10
CBC8	38	39	116	117	118	115	114	119	159	162	163	160	164	166	165	161	21	23	20
CBC9	11	12	39	40	41	42	43	44	42	45	46	43	47	49	48	44	5	9	9
CBC10	36	37	110	111	112	109	108	113	158	157	151	155	152	149	150	156	20	22	19
CBC11	9	10	33	34	35	36	37	38	34	37	38	35	39	41	40	36	4	8	8
CBC12	33	34	103	104	105	102	101	106	133	136	137	134	138	140	139	135	19	21	18
CBC13	7	8	27	29	29	30	31	32	25	29	30	27	31	33	32	28	3	7	7
CBC14	31	32	97	98	99	96	95	100	125	128	129	126	130	132	131	127	18	20	17
CBC15	5	6	21	22	23	24	25	26	18	21	22	19	23	25	24	20	2	6	6
CBC16	29	30	91	92	93	90	89	94	124	123	119	121	120	117	118	122	17	19	16

Figure 14-6.
Channel Buffer-Clamp ("CBC") Circuit Schematic Diagram



Note

Detail table for general circuit schematic shows actual component designations used for each circuit. Component values (such as ohms) are shown in schematic. Small, simplified diagram, located below schematic, shows the input/output connections for general circuit.

"ØSC' Detail Table

REF DES	CA	CB	CC	CD	CE	CF	CG	CH	CJ	RA	RB	RC	RD	RE	RF	RG	RH	RJ	RK	RL	RM	OR	OB	CRA	UA	TBA	TPB
OSC1	408	414	413	410	409	416	411	415	412	527	529	533	532	537	536	535	528	534	531	530	538	68	67	37	70	99	97
OSC2	405	403	407	400	406	465	399	402	398	526	524	521	522	494	518	519	525	520	523	489	517	66	65	36	68	95	96
OSC3	378	384	404	380	379	386	381	385	382	486	487	493	492	497	496	495	488	490	491	485	501	64	63	35	66	92	91
OSC4	375	373	377	370	376	371	369	372	368	478	479	482	481	467	499	498	483	484	480	474	466	62	61	34	64	89	90
OSC5	348	354	374	350	349	356	351	355	352	477	476	472	471	445	469	468	475	473	470	433	446	60	59	33	62	88	86
OSC6	346	344	347	322	345	342	327	343	329	432	436	437	438	414	440	441	435	434	439	427	442	58	57	32	60	84	85
OSC7	316	319	318	314	317	321	313	320	312	382	383	387	386	396	394	393	384	388	385	381	395	50	49	31	57	81	82
OSC8	292	297	315	294	293	299	295	298	296	378	379	372	373	362	369	370	380	371	374	376	368	48	47	30	55	79	80
OSC9	289	288	291	271	290	286	270	287	272	323	324	336	335	338	360	361	377	375	334	325	337	46	45	29	53	76	77

Figure 14-7.
Phase-Shifting Clamp ("ΦSC") Circuit Schematic Diagram

14-15 Effects Processor

The Effects Processor contains the logic that generates the control signals for the four video multipliers, to produce the signal for the output amplifier. It consists of cascaded AND and OR gates which mix the various A, B, Insert, and Key video control signal combinations. The effects key is set up as a downstream keyer over the A bus and B bus. The three control outputs (A, B, and Insert) go into the video multipliers to produce the output video signals. Software ensures that the sum of the A, B, Insert, and Black control signals is unity.

14-16 FUSES, TEST POINTS, AND JUMPERS

The following paragraphs describe the fuses, test points and jumpers.

14-17 Fuses

The Component Video Switcher PWA has one fuse, F1 (P/N 070-443), rated at 5.0 amp. The fuse is soldered to two posts (see Figure 14-1 for location of fuse). Replace fuse with equivalent fuse.

14-18 Test Points

Table 14-1 lists the test points and their associated signals.

14-19 Jumpers

Table 14-2 lists jumpers and their functions. Refer to Figure 14-1 for the location of jumpers on the Component Video Switcher PWA.

Jumpers J5 through J48 set delay times for video signals. Delay times are measured and set at the factory; these jumpers normally should not be changed.

Jumper J49 selects between a constant dc level out on the Black video signal, or Sync/Composite Blanking (SMPTE standard) on the Black signal.

Jumper J50 selects between Ground (all standards except SMPTE) and Sync/Composite Blanking (SMPTE standard).

14-20 ADJUSTMENTS

The following paragraphs describe the test equipment and adjustments that are performed on the Component Video Switcher PWA.

14-21 Test Equipment

Table 14-3 lists the recommended test equipment for performing adjustments on the Component Video Switcher PWA.

Table 14-1. Component Video Switcher PWA Test Points

Test Point	Signal
TP1	–12V
TP2	+12V
TP3	KEY1 (Key Input to "CBC" circuit)
TP4	KEY1C (Not Mounted) (Key output from "CBC" circuit)
TP5	PR5 (Pr5 input to "CBC" circuit)
TP6	PR5C (Pr5 output from "CBC" circuit)
TP7	PR3 (Pr3 input to "CBC" circuit)
TP8	PR3C (Pr3 output from "CBC" circuit)
TP9	PR1 (Pr1 input to "CBC" circuit)
TP10	PR1C (Pr1 output from "CBC" circuit)
TP11	PB5 (Pb5 input to "CBC" circuit)
TP12	PB5C (Pb5 output from "CBC" circuit)
TP13	PB3 (Pb3 input to "CBC" circuit)
TP14	PB3C (Pb3 output from "CBC" circuit)
TP15	PB1 (Pb1 input to "CBC" circuit)
TP16	PB1C (Pb1 output from "CBC" circuit)
TP17	Y6 (Y6 input to "YBC" circuit)
TP18	Y6C (Y6 output from "YBC" circuit)
TP19	Y4 (Y4 input to "YBC" circuit)
TP20	Y4C (Y4 output from "YBC" circuit)
TP21	Y2 (Y2 input to "YBC" circuit)
TP22	Y2C (Y2 output from "YBC" circuit)
TP23	Y1 (Y1 input to "YBC" circuit)
TP24	Y1C (Y1 output from "YBC" circuit)
TP25	DGND (Digital Ground)
TP26	DGND (Digital Ground)
TP27	+5V
TP28	AGND (Analog Ground)
TP29	PR6 (Pr6 input to "CBC" circuit)
TP30	PR6C (Pr6 output from "CBC" circuit)

(Continued next page)

Table 14-1. Component Video Switcher PWA Test Points (Continued)

Test Point	Signal
TP31	PR4 (Pr4 input to "CBC" circuit)
TP32	PR4C (Pr4 output from "CBC" circuit)
TP33	PR2 (Pr2 input to "CBC" circuit)
TP34	PR2C (Pr2 output from "CBC" circuit)
TP35	AGND (Analog Ground)
TP36	PB6 (Pb6 input to "CBC" circuit)
TP37	PB6C (Pb6 output from "CBC" circuit)
TP38	PB4 (Pb4 input to "CBC" circuit)
TP39	PB4C (Pb4 output from "CBC" circuit)
TP40	PB2 (Pb2 input to "CBC" circuit)
TP41	PB2C (Pb2 output from "CBC" circuit)
TP42	AGND (Analog Ground)
TP43	Y5 (Y5 input to "YBC" circuit)
TP44	Y5C (Y5 output from "YBC" circuit)
TP45	Y3 (Y3 input to "YBC" circuit)
TP46	Y3C (Y3 output from "YBC" circuit)
TP47	BLK (Black input to "YBC" circuit)
TP48	BLKC (Black output from "YBC" circuit)
TP49	PRI
TP50	PRB
TP51	PRA
TP52	AGND (Analog Ground)
TP53	PBI (output of Pb Insert Crosspoint Matrix)
TP54	PBB (output of Pb B Crosspoint Matrix)
TP55	PBA (output of Pb A Crosspoint Matrix)
TP56	YI (ouput of Y Insert Crosspoint Matrix)
TP57	AGND (Analog Ground)
TP58	YB (output of Y B Crosspoint Matrix)
TP59	YA (output of Y A Crosspoint Matrix)
TP60	YBLK (output of Y Black Crosspoint Matrix)

(Continued next page)

Table 14-1. Component Video Switcher PWA Test Points (Continued)

Test Point	Signal
TP61	DGND (Digital Ground)
TP62	PR KEY (Pr Key into "CBC" circuit)
TP63	CKEY (Chroma Key)
TP64	PBKEY (Pb Key into "CBC" circuit)
TP65	-AK MIX
TP66	-BK MIX
TP67	INS VID CTRL
TP68	B MIX
TP69	KEY (Luminance Key)
TP70	A VIDEO CTRL
TP71	INS KEY (Insert Key Video)
TP72	BKG KEY (Background Key VIdeo)
TP73	VID CTR
TP74	A MIX
TP75	PR OUT (Pr Channel output)
TP76	PRI (Pr I input to "ΦSC" circuit)
TP77	PRI VIDC (Pr I output from "ΦSC" circuit)
TP78	A GND (Analog Ground)
TP79	PR B (Pr B input to "ΦSC" circuit)
TP80	PR B VIDC (Pr B output from "ΦSC" circuit)
TP81	PR A VID (Pr A input to "ΦSC" circuit)
TP82	PR A VIDC (Pr A output from "ΦSC" circuit)
TP83	PB OUT (Pb Channel output)
TP84	PB I (Pb I input to "ΦSC" circuit)
TP85	PBI VIDC (Pb I output from "ΦSC" circuit)
TP86	PB B VIDC (Pb B output from "ΦSC" circuit)
TP87	AGND (Analog Ground)
TP88	PB B VID (Pb B input to "ΦSC" circuit)
TP89	PB A VID (Pb A input to "ΦSC" circuit)
TP90	PB A VIDC (Pb A output from "ΦSC" circuit)

(Continued next page)

Table 14-1. Component Video Switcher PWA Test Points

Test Point	Signal
TP91	Y1 VIDC (Y1 output from "ΦSC" circuit)
TP92	Y1 VID (Y1 input to "ΦSC" circuit)
TP93	–K B MIX
TP94	INS MIX
TP95	YB VID (Y B input to "ΦSC" circuit)
TP96	YB VIDC (Y B output from "ΦSC" circuit)
TP97	YA VIDC (Y A output from "ΦSC" circuit)
TP98	YA VID (Y A input to "ΦSC" circuit)
TP99	AGND (Analog Ground)
TP100	Y BLK VID (Y Black input to "CBC" circuit)
TP101	Y BLK VIDC (Y Black output from "CBC" circuit)
TP102	NOT USED
TP103	NOT MOUNTED (Pb Key out from "CBC" circuit)
TP104	NOT MOUNTED (Pr Key out from "CBC" circuit)
TP105	BLK VID CNTR
TP106	AGND (Analog Ground)
TP107	Y OUT (Y Channel output)

Table 14-2. Component Video Switcher PWA Jumpers

Jumper	Description
J5	10 ns Key Video Delay
J6	20 ns Key Video Delay
J7	40 ns Key Video Delay
J8	80 ns Key Video Delay
J9	80 ns Pr Insert Video Delay
J10	40 ns Pr Insert Video Delay
J11	20 ns Pr Insert Video Delay
J12	10 ns Pr Insert Video Delay
J13	80 ns Pr B Video Delay
J14	40 ns Pr B Video Delay
J15	20 ns Pr B Video Delay
J16	10 ns Pr B Video Delay
J17	80 ns Pr A Video Delay
J18	40 ns Pr A Video Delay
J19	20 ns Pr A Video Delay
J20	10 ns Pr A Video Delay
J21	80 ns Pb Insert Video Delay
J22	40 ns Pb Insert Video Delay
J23	20 ns Pb Insert Video Delay
J24	10 ns Pb Insert Video Delay
J25	80 ns Pb B Video Delay
J26	40 ns Pb B Video Delay
J27	20 ns Pb B Video Delay
J28	10 ns Pb B Video Delay
J29	80 ns Pb A Video Delay
J30	40 ns Pb A Video Delay
J31	20 ns Pb A Video Delay
J32	10 ns Pb A Video Delay

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Table 14-2. Component Video Switcher PWA Jumpers (Continued)

Jumper	Description
J33	80 ns Insert Bus Delay
J34	40 ns Insert Bus Delay
J35	20 ns Insert Bus Delay
J36	10 ns Insert Bus Delay
J37	80 ns B Bus Delay
J38	40 ns B Bus Delay
J39	20 ns B Bus Delay
J40	10 ns B Bus Delay
J41	80 ns A Bus Delay for Key Channel
J42	40 ns A Bus Delay for Key Channel
J43	20 ns A Bus Delay for Key Channel
J44	10 ns A Bus Delay for Key Channel
J45	80 ns Y Blk Video Delay
J46	40 ns Y Blk Video Delay
J47	20 ns Y Blk Video Delay
J48	10 ns Y Blk Video Delay
J49	Position 2-3: (dc) Constant dc level out on Black (0.5 Vdc for non-sync)
J49	Position 1-4: (SCB) Sync and Composite Blanking on Black (SMPTE Standard)
J50	Position 1-2: (GND) All standards (except SMPTE)
J50	Position 3-4: (SCB) Sync/Composite Blanking (SMPTE)

Table 14-3. Recommended Test Equipment

Equipment	Recommended Model
Oscilloscope	Tektronix 465A or equivalent
Video Signal Generator	Tektronix140 or equivalent
Video Signal Generator	Tektronix 147 or equivalent
Video Signal Generator	Tektronix TSG300 or equivalent
Probe, Oscilloscope (2)	Tektronix 6106 or equivalent
Waveform Monitor	Tektronix 1485R or equivalent
Waveform Monitor	Tektronix WFM 300 or equivalent
Color Monitor	Tektronix 655HR or equivalent
Vectorscope	Tektronix 5208 or equivalent
Video Distribution System	Dynair 5300 or equivalent
Cable, coax, BNC connector, 75Ω (25 required)	

14-22 Power Supply Checks

Check the following points for the corresponding voltages:

TP1 −12V ±0.6V

TP2 +12V ±0.6V

TP27 +5V ±0.25V

If R221 is installed, adjust this pot for +3 Vdc measured at U31, pin 7.

14-23 Bus Verification

The following procedure is used to verify that the crosspoint bus operates correctly.

1. Use the composite white signal out of the 147 Preview Generator. Set the program control switch to AUXILIARY and the REMOTE/LOCAL switch to LOCAL. Set the AUXILIARY PEDESTAL for the white level at 100 IRE.

2. Connect AT-style keyboard to ACE 25 Edit Controller to run diagnostics and enter commands.

3. Press Shift F10 to clear the switcher.

4. Select the A bus (A Bus Level: FF).

5. Verify that all of the crosspoints are operational. Press F1 to sequence through the following crosspoints:

   A Bus Crosspoint: FD (Composite Multiburst)

   A Bus Crosspoint: FE (Reference Black)

   A Bus Crosspoint: BF (Composite Ramp)

   A Bus Crosspoint: DF (Component Multiburst)

   A Bus Crosspoint: EF (Component Color Bars)

   A Bus Crossopint: F7 (Composite White)

   A Bus Crosspoint: FB (Composite Color Bars)

6. Push the "+" key and press Shift F1 until B Bus Level: FF is selected (the B bus).

7. Verify all of the crosspoints are operational. Press F2 to sequence through the following crosspoints:

   B Bus Crosspoint: FD (Composite Multiburst)

   B Bus Crosspoint: FE (Reference Black)

   B Bus Crosspoint: BF (Composite Ramp)

   B Bus Crosspoint: DF (Component Multiburst)

   B Bus Crosspoint: EF (Component Color Bars)

   B Bus Crosspoint: F7 (Composite White)

   B Bus Crosspoint: FB (Composite Color Bars)

8. Press F9, then press F4 until Key Clip: 00 is selected (the KEY Bus).

9. Verify that all of the crosspoints are operational. Press F10 to sequence through the following crosspoints:

   KEY Bus Crosspoint: FD (Composite Multiburst)

   KEY Bus Crosspoint: FE (Reference Black)

   KEY Bus Crosspoint: BF (Composite Ramp)

   KEY Bus Crosspoint: DF (Component Multiburst)

   KEY Bus Crosspoint: EF (Component Color Bars)

   KEY Bus Crosspoint: F7 (Composite White)

   KEY Bus Crosspoint: FB (Composite Color Bars)

14-24 Y Channel Bus Adjustments

Note

Use Composite Video for the following tests. Set unity gain using waveform monitor.

1. Connect Y 2 OUT to COMPOSITE VIDEO IN signal from test rack.
2. Set the generator to ramp.
3. With the switcher out of the loop, adjust Distribution Amplifier to match the video gain to the calibrated pulse out of the waveform monitor (cables joined together).
4. Set the generator to multiburst and make a reference of the waveform monitor (terminated) with the lowest vertical gain setting.
5. Reconnect the cables to the switcher.
6. Connect scope Channel 1 to TP107 (Y CHANNEL OUT) unterminated.
7. Press Shift F10.
8. Set the generator to ramp.
9. Adjust YA GAIN pot (R544) for unity again. This is done by matching the calibrated pulse to the video ramp ±0.1 IRE.
10. Set the generator to multiburst.
11. Adjust the YA HF capacitor (C420) to center of frequency response range.
12. Adjust Y OA HF capacitor (C439) for frequency response to be equal to waveform monitor reference ±1 IRE.
13. Adjust YA dc pot (R511) for the back porch to be at 0 Vdc ±2 mV.

14. Push "+" key to select the Turbo mode, then press the Shift F1 key until B Bus Level: FF is selected.

15. Set the generator to ramp.

16. Adjust YB GAIN pot (R509) for unity gain. This is done by matching the calibrated pulse to video ramp ±0.1 IRE.

17. Set the generator to multiburst.

18. Adjust YB HF cap (C393) for frequency reponse to equal waveform monitor reference ±1 IRE.

19. Adjust YB dc pot (R508) for back porch to be at 0 Vdc ±2 mV.

20. Set the generator to ramp.

21 Press F9.

22. Adjust YI GAIN pot (R506) for unity gain. This is done by matching the calibrated pulse to video ramp ±0.1 IRE.

23. Set the generator to multiburst.

24. Adjust YI HF cap (C390) for frequency response to equal waveform monitor reference ±1 IRE.

25. Adjust YI dc pot (R460) for back porch to be at 0 Vdc ±2 mV.

14-25 Y Channel Transition Adjustments

To adjust Y Channel for A to B Transitions:

1. Press Shift F10, then Shift F5.

2. Adjust the B MIX LIN pot (R238) for minimum frequency response dip during the transitions. Signal dip should be less than ±1 IRE.

3. Adjust YB TRANS pot (R510) for dc disturbances to be less than ±10 mV (unterminated) measured at back porch.

To adjust Y Channel for A to INSERT Transitions:

1. Press Shift F10, then CTRL F1.

2. Adjust INS MIX LIN pot (R256) and AK MIX LIN pot (R270) for minimum frequency response dip during transitions. Dip should be less than ±1 IRE.

Note

These two adjustments should end up with both pots off the end stops by approximately the same amount.

3. Adjust YI TRANS pot (R507) for dc disturbances to be less than ±1 IRE.

4. The insert switching glitches on the front and back porch should be less than ±20 mV (unterminated).

To adjust Y Channel for A to Black Transitions:

1. Press Shift F10.
2. Press F1 until A Bus Crosspoint: FE is selected.
3. Press F2 until B Bus Crosspoint: FE is selected.
4. Press Shift F7.
5. Adjust YBLK dc pot (R546) for back porch to be at 0 Vdc ±2 mVdc.
6. Adjust YBLK TRAN pot (R548) and BLK FADE LIN pot (R255) for minimum dc transition disturbances. The dc disturbances should be less than ±10 mVdc (unterminated).
7. Adjust YBLK GAIN pot (R547) for the Black amplitudes to be the same (±5 mV).

Note
Black gains are adjusted by matching setups.

To adjust Y Channel for B to Black Transitions:

1. Press shift bar on the keyboard.
2. Press Shift F8.
3. Verify dc transition disturbances are less than ±10 mVdc (unterminated). If they are not, adjust YBLK TRAN pot (R548) and BLK FADE LIN pot (R255). If either adjustment is made, recheck the A to Black Transitions.

Note
Use Composite Black Burst to set up BLK FADE LIN pot and Black Frequency Response.

To adjust Y Channel for B to INSERT Transitions:

1. Press Shift F10, then CTRL F2.
2. Adjust BK MIX LIN pot (R280) for minimum frequency response dip during transitions. Dip should be less than ±1 IRE. If a slight adjustment of INS MIX LIN pot (R256) is necessary, recheck A to INSERT Transitions.
3. Verify dc transition disturbances are less than ±10 mVdc (unterminated). If they are not, split the errors with A to INSERT Transitions. If they are still out, adjust the YA TRANS pot (R545) and YB TRANS pot (R510) and redo the Y Channel Transition adjustments.
4. Insert switching signal disturbances on front porch and back porch should be less than ±20 mV (unterminated).

14-26 Pb Channel Bus Adjustments

The following procedure is used to adjust the Pb Channel Bus:

1. Connect PB 2 OUT to COMPOSITE VIDEO OUT.
2. Set the generator to ramp.
3. With the switcher out of the loop adjust Distribution Amplifier to match the video gain to the calibrated pulse out of the waveform monitor (cables barelled together).
4. Set the generator to multiburst and make a reference on waveform monitor using lowest vertical setting.
5. Press Shift F10.
6. Set the generator to ramp.
7. Adjust PBA GAIN pot (R458) for unity gain. This is done by matching the calibrated pulse to video ramp ±0.1 IRE.
8. Set the generator to multiburst.
9. Adjust PBA HF cap (C363) to center of frequency response range.
10. Adjust PB OA HF cap (C440) for frequency response to equal waveform monitor reference ±1 IRE.
11. Adjust PBA dc pot (R457) for back porch to be at 0 Vdc ±2 mV.
12. Push "+" key and press shift F1 key until B Bus Level: FF is selected.
13. Set the generator to ramp.
14. Adjust PBB GAIN pot (R455) for unity gain. This is done by matching the calibrated pulse to video ramp ±0.1 IRE.
15. Set the generator to multiburst.
16. Adjust PBB HF cap (C360) for frequency response to equal waveform monitor reference ±1 IRE.
17. Adjust PBB dc pot (R454) for back porch to be at 0 Vdc ±2 mV.
18. Set the generator to ramp.
19. Press F9.
20. Press F4 until Key Clip: 00 is selected.
21. Adjust PBI GAIN pot (R452) for unity gain. This is done by matching the calibrated pulse to video ramp ±0.1 IRE.
22. Set the generator to multiburst.

23. Adjust PBI HF cap (C337) for frequency reponse to equal waveform monitor reference ±1 IRE.

24. Adjust PBI dc pot (R410) for back porch to be at 0 Vdc ±2 mV.

14-27 Pb Channel Transition Adjustments

To adjust the Pb Channel for A to B Transitions:

1. Press Shift F10, then Shift F5.

2. Verify frequency response dip during transitions is less than ±1 IRE. If the frequency response dip is more than ±1 IRE, the B MIX LIN pot (R238) may be adjusted and Y Channel A to B Transitions rechecked.

3. Adjust PBB TRANS pot (R456) for dc disturbances to be less than ±10 mV (unterminated) measured from back porch.

To adjust the Pb Channel for A to INSERT Transitions:

1. Press Shift F10, then CTRL F1.

2. Verify frequency response dip during transitions is less than ±1 IRE. If frequency response dip is more than ±1 IRE, the INS MIX LIN pot (R256) and AK MIX LIN pot (R270) may be adjusted and Y Channel A to INSERT Transitions rechecked.

Note

These two adjustments should end up with both pots off the end stops by approximately the same amount.

3. Adjust PB I TRANS pot (R453) for dc disturbances to be less than ±1 IRE.

4. The insert switching signal disturbances on front porch and back porch should be less than ±20 mV (unterminated).

To adjust the Pb Channel for A to Black Transitions:

1. Press Shift F10.

2. Press F1 until A Bus Crosspoint: FE is selected.

3. Press F2 until B Bus Crosspoint: FE is selected.

4. Press Shift F7.

5. Adjust PB BLK dc pot (R407) for back porch to be 0 Vdc ±5 mVdc.

6. Adjust PB BLK TRAN pot (R409) for minimum dc transition disturbances. The dc disturbances should be less than ±10 mVdc (unterminated). If they are not less than ±10 mVdc, a slight adjustment of BLK FADE LIN (R255) may be necessary. If BLK FAD LIN is adjusted, recheck Y Channel A to Black Transitions.

7. Adjust PBBLK GAIN pot (R408) for Black amplitudes to be the same (±5 mV).

Note

Black gains are adjusted by matching setups.

To adjust the Pb Channel for B to Black Transitions:

1. Press space bar on keyboard.

2. Press Shift F8.

3. Verify dc transition disturbances are less than ±10 mVdc (unterminated). If they are not, adjust PBBLK TRAN pot (R548). If this adjustment is made, recheck the A to Black Transitions.

Note

As a last resort, adjust BLK FADE LIN pot (R255). If this adjustment is made, recheck the Y Channel A and B to Black Transitions.

Use composite black burst to set up BLK FADE LIN pot and Black Frequency Response.

To adjust the Pb Channel for B to INSERT Transitions:

1. Press Shift F10, then CTRL F2.

2. Verify frequency response dip during transitions is less than ±1 IRE. If frequency response dip is more than ±1 IRE, a slight adjustment of the BK MIX LIN pot (R280) may be necessary. If BK MIX LIN adjustment is made, recheck the Y Channel B to INSERT Transitions.

3. Verify dc transition disturbances are less than ±10 mV (unterminated). If they are not, split errors with the A to INSERT Transitions. If the specification is still not met, adjust PB A TRANS pot (R459) and PB B TRANS pot (R456), and redo the PB Channel Transition adjustments.

4. The insert switching signal disturbances on front porch and back porch should be less than ±20 mV (unterminated).

14-28 Pr Channel Bus Adjustments

The following procedure is used to adjust the Pr Channel Bus:

1. Connect PB 2 OUT to COMPOSITE VIDEO IN from the test rack.

2. Set the generator to ramp.

3. With the switcher out of the loop, adjust distribution amplifier to match the video gain to the calibrated pulse out of the waveform monitor (cables joined together).

4. Set the generator to multiburst and make a reference on the waveform monitor using lowest vertical setting.

5. Press Shift F10.

6. Set the generator to ramp.

7. Adjust PR A GAIN pot (R405) for unity gain. This is done by matching calibrated pulse to video ramp ±0.1 IRE.

8. Adjust PR A HF cap (C307) to center of frequency response range.

9. Adjust PR OA HF cap (C273) for frequency response to equal waveform monitor reference ±1 IRE.

10. Adjust PR A dc pot (R404) for back porch to be at 0 Vdc ±2 mV.

11. Push the "+" key and press shift F1 key until B Bus Level: FF is selected.

12. Set the generator to ramp.

13. Adjust PR B GAIN pot (R402) for unity gain. This is done by matching the calibrated pulse to video ramp ±0.1 IRE.

14. Set the generator to multiburst.

15. Adjust PR B HF cap (C304) for frequency response to equal waveform monitor reference ±1 IRE.

16. Adjust PR B dc pot (R354) for back porch to be at 0 Vdc ±2 mV.

17. Set the generator to ramp.

18. Press F9.

19. Press F4 until Key Clip: 00 is selected.

20. Adjust PR I GAIN pot (R352) for unity gain. This is done by matching calibrated pulse to video ramp 0.1 IRE.

21. Set the generator to multiburst.

22. Adjust PR I HF cap (C281) for frequency response to equal waveform monitor reference ±1 IRE.

23. Adjust PR I dc pot (R351) for back porch to be 0 Vdc ±2 mV.

14-29 Pr Channel Transition Adjustments

To adjust the Pr Channel for A to B Transitions:

1. Press Shift F10, then Shift F5.
2. Verify frequency response dip during transitions is less than ±1 IRE. If frequency response dip is more than ±1 IRE, the B MIX LIN pot (R238) may be adjusted and the Y Channel and Pb Channel A to B Transitions rechecked.
3. Adjust PR B TRANS pot (R402) for dc disturbances to be less than ±10 mV (unterminated) measured from back porch.

To adjust the Pr Channel for A to INSERT Transitions:

1. Press Shift F10, then CTRL F1.
2. Verify frequency response dip during transitions is less than ±1 IRE. If the frequency response dip is more than ±1 IRE, the INS MIX LIN pot (R256) and AK MIX LIN pot (R270) may be adjusted, and the Y and Pr Channels A to INSERT Transitions rechecked.

Note

These two adjustments should end up with both pots off the end stops by approximately the same amount.

3. Adjust PR I TRANS pot (R353) for dc disturbances to be less than ±1 IRE.
4. The insert switching signal disturbances on front porch and back porch should be less than ±20 mV (unterminated).

To adjust the Pr Channel for A to Black Transitions:

1. Press Shift F10.
2. Press F1 until A Bus Crosspoint: FE is selected.
3. Press F2 until B Bus Crossopoint: FE is selected.
4. Press Shift F7.
5. Adjust PR BLK dc pot (R348) for back porch to be at 0 Vdc ±2 mVdc.
6. Adjust PR BLK TRAN pot (R350) for minimum dc transition disturbances. The dc disturbances should be less than ±10 mVdc (unterminated). If they are not less than ±10 mVdc, a slight adjustment of BLK FADE LIN (R255) may be necessary. If BLK FADE LIN is adjusted, recheck Y Channel and PR Channel A to Black Transitions.

7. Adjust YBLK GAIN pot (R349) for the black amplitudes to be the same (±5 mV).

Note

Black gains are adjusted by matching setups.

To adjust the Pr Channel for B to Black Transitions:

1. Press space bar on keyboard.
2. Press Shift F8.
3. Verify dc transition disturbances are less than ±10 mVdc (unterminated). If they are not, adjust PRBLK TRAN pot (R350). If this adjustment is made, recheck the A to Black Transitions.

Note

As a last resort, adjust BLK FADE LIN pot (R255). If this adjustment is made, recheck Y Channel A to Black, Y Channel B to Black, PB Channel A to Black, PB Channel B to Black, and PR Channel A to Black Transitions.

To adjust the Pr Channel for B to INSERT Transitions:

1. Press Shift F10, then CTRL F2.
2. Verify frequency response dip during transitions is less than ±1 IRE. If the frequency response dip is more than ±1 IRE, a slight adjustment of BK MIX LIN pot (R280) may be necessary. If a BK MIX LIN adjustment is made, recheck the Y Channel and PB Channel B to INSERT Transitions.
3. Verify the dc transition disturbances are less than ±10 mV (unterminated). If they are not, split the errors with the A to INSERT Transitions. If they are still out, adjust PRA TRANS pot (R406) and PRB TRANS pot (R402), and repeat the PR Channel Transition adjustments.
4. The insert switching signal disturbances on front porch and back porch should be less than ±20 mV (unterminated).

14-30 Chroma Key Adjustments

To adjust the Chroma Key for PB/PR Gain Adjustments:

Note

Use component color bars for the following adjustments.

1 Press Shift F10.

2. Select the crosspoint with color bar input. Set oscilloscope probe to output of B crosspoint selected (e.g., TP36), for the input signal to oscilloscope clamp.
3. Set oscilloscope to 50 mV/DIV and verify amplitude is 350 mV (700 mV peak-to-peak). This is Beta Color Bars.

4. Press ALT F3 (to set switcher to SIN ON and COS OFF).

5. Attach oscilloscope to TP63.

6. Press F10 to select KEY Bus crosspoint with color bar signal.

7. Adjust PB GAIN pot (R285) for a gain of 2 ±10 mV (700 mV on the 100 mV scale, center to peak).

8. Press ALT F4 (to set switcher to SIN OFF and COS ON).

9. Adjust PR GAIN pot (R248) for a gain of 2 ±10 mV (700 mV on the 100 mV scale, center to peak).

To adjust the Chroma Key for SIN/COS Null Adjustments:

1. Press ALT F7 (to set switcher to SIN OFF and COS OFF).

2. Adjust the SIN and COS NULL puts (R273 and R243) for minimum signal. Signal should be less than 10 mV peak-to-peak.

Note

PB/PR GAIN adjustments and SIN/COS NULL adjustments interact and must be repeated until all are within specification.

3. Set the generator for multiburst and verify frequency response at TP63 is flat from +0 to ±20 IRE.

To adjust Chroma Key Hues:

1. Press ALT F3.

2. Press and hold ALT F1 or ALT F2 and monitor TP63.

3. Rotate 360° (00 through FF).

4. Verify crankshaft signal on TP63 never has more than a gain of two.

Note

ALT F1 equals chroma key hue "+" and ALT F2 equals chroma key hue "-".

5. Press Shift F10.

6. Select A Bus Crossoint: FE with F1. Select KEY Bus Crosspoint: FB (Color Bar crosspoint) with F10.

7. Press F9 (KEY Initialize).

8. Press F7 to select CHROMA KEY.

9. Set Key Gain: 04 with F5 and F6.

10. Adjust Key Clip Level with F3 and F4 until only one bar of color bar signal is present on color monitor.

11. Press and hold ALT F1. Verify that one color bar at a time appears and disappears on color monitor as the signal is rotated.

To adjust Chroma Key Clip:

1. Connect oscilloscope probe to TP69.

2. Press Shift F10, then press F9.

3. Press F10 until KEY Bus Crosspoint: FB is selected (Color Bars).

4. Press "+" for Turbo mode.

5. Press F5 to set Key Gain: 00.

6. Press F3 and F4 to set the Key Clip from 00 to FF. With Key Clip at 00, key signal at TP69 should be + 0.3 V ±0.1 V.

7. With Key Clip at FF, key signal at TP69 should be at -2.8 V ±0.1 V.

8. Press "–" to turn Turbo mode off.

9. Connect oscilloscope probe to Y Channel Out (TP107). Set vertical gain to maximum.

10. By pressing Key Clip (F3 and F4), verify that there are seven counts of dead zone (00-07) at low end, and seven counts of dead zone at high end (F8-FF).

11. Connect oscilloscope probe to INS KEY (TP71).

12. With Key Clip at 00, dc level should be at least +2.3 V.

13. With Key Clip at FF, dc level should be at least ±0.2 V.

14-31 Timing

To adjust Y Channel Timing, the YI, YA, and YB Timing adjustments are performed. The YI Timing sets the reference phase for the entire ACE 25 system.

Note

Timing is done with composite 2T signal keyed over composite white signal. Composite white signal comes from 147 Preview Generator. Set program control switch to AUXILIARY, and REMOTE/LOCAL switch to LOCAL. Set AUXILIARY PEDESTAL to have white level at 100 IRE.

To adjust the Y Channel for YI Timing:

1. Connect oscilloscope to TP107 (Y CHANNEL OUT).

2. Set color monitor to NTSC.

3. Set the 147 Full Field Generator to 2T signal.

4. Press Shift F10.

5. Set A Bus Crosspoint: F7 (white video) with F1.

6. Set B Bus Crosspoint: F7 (white video) with F2.

7. Set KEY Bus Crosspoint: FD (2T video) with F10.

8. Press F9 (Key Initialize).

9. Press F7 to select Chroma Key.

10. Connect oscilloscope to TP63, and monitor video.

11. Press ALT F1 and/or ALT F2 for the most positive-going 2T pulse.

Note

ALT F1 is Chroma Key Hue "+" and ALT F2 is Chroma Key Hue "-".

12. Set KEY Gain: 03 with F5 and F6.

13. Press "+" for the Turbo mode.

14. Set KEY Clip: 40 with F3 and F4.

15. Press the "–" on the keyboard to leave the Turbo mode.

16. Fine tune the KEY Clip.

Note

This is done using X20 horizontal magnification on waveform monitor.

17. While looking at the picture monitor, adjust YI phase shifter (R490) to visually center the 2T pulse in the key hole. If the 2T pulse can not be centered in key hole, reset jumpers for YI delay line (DL 8). If delay line jumpers are reset, all Y Channel adjustments must be redone.

18. Press F7 (Key Source Select) and verify 2T video is present with all three key sources.

Note

Composite 2T signal must be connected to external key input.

19. Rotate through the three selections and balance setting of R490 for best overall picture.

To adjust the Y A Timing:

1. Set the 147 Generator for composite ramp.

2. Set vectorscope Phase REF to EXT.

3. Press Shift F10, then F9.

4. Press "+" for the Turbo mode.

5. Set KEY Clip Level: 00 with F4.

6. Set reference phase on outer calibration circle while monitoring YI on vectorscope.

7. Press Shift F10 (A Bus selected).

8. Adjust YA PHASE pot (R534) for signal to match phase reference.

9. If phase pot can not be adjusted to match reference, reset YA Delay Line (DL 10) jumpers.

10. If delay line jumpers are reset, redo all Y Channel adjustments.

To adjust the Y B Timing:

1. Select B Bus by pressing Shift F1 until B Bus Level: FF is reached.

2. Adjust YB PHASE pot (R520) for the signal on vectorscope to match reference phase.

3. If phase pot can not be adjusted to match reference, reset YB Delay Line (DL 9) jumpers.

4. If delay line jumpers are reset, redo all Y Channel adjustments.

14-32 Pb Channel Timing

To adjust the Pb A Timing:

Note

Have all test equipment monitor PB Channel output.

1. Press Shift F10.

2. Adjust PB A PHASE pot (R484) for signal to match phase reference.

3. If phase pot can not be adjusted to match reference, reset PB A delay line (DL 7) jumpers.

4. If delay line jumpers are reset, redo all PB Channel adjustments.

To adjust the Pb B Timing:

1. Select B Bus by pressing Shift F1 until B Bus Level: FF is reached.

2. Adjust PB B PHASE pot (R473) for signal to match phase reference.

3. If phase pot can not be adjusted to match reference, reset PB B Delay Line (DL 6) jumpers.

4. If delay line jumpers are reset, redo all Pb Channel adjustments.

To adjust the Pb I Timing:

1. Press F9 (Key Init).
2. Press F4 to set Key Clip: 00.
3. Adjust PB I PHASE pot (R434) for signal to match phase reference.
4. If phase pot can not be adjusted to match reference, reset PB I Delay Line (DL 5) jumpers.
5. If delay line jumpers are reset, redo all Pb Channel adjustments.

14-33 Pr Channel Timing

To adjust Pr Channel Timing, the following procedures are performed:

Note
Have all of the test equipment monitor Pr Channel output.

To adjust Pr A Timing:

1. Press Shift F10.
2. Adjust PR A PHASE pot (R388) for signal to match phase reference.
3. If phase pot can not be adjusted to match reference, reset Pr A Delay Line (DL 4) jumpers.
4. If delay line jumpers are reset, redo all Pr Channel adjustments.

To adjust Pr B Timing:

1. Select B Bus by pressing Shift F1 until B Bus Level: FF is reached.
2. Adjust PR B PHASE pot (R371) for signal to match phase reference.
3. If phase pot can not be adjusted to match reference, reset Pr B Delay Line (DL 3) jumpers.
4. If delay line jumpers are reset, redo all Pr Channel adjustments.

To adjust Pr I Timing:

1. Press F9 (Key Initialize).
2. Press F4 to set KEY Clip: 00.
3. Adjust PR I PHASE pot (R375) for signal to match phase reference.
4. If phase pot can not be adjusted to match reference, reset Pr I Delay Line (DL 2) jumpers.
5. If delay line jumpers are reset, redo all Pr Channel adjustments.

14-34 Black Timing

To adjust Black Timing, the following procedures are performed:

1. Attach oscilloscope Channel 1 to TP47 (Black In) and Channel 2 to TP23 (Y1 In).
2. Adjust Video Timing Generator PWA H Phase pot (R18) to make leading edges of H sync to be coincident at the 50 points.
3. Connect oscilloscope Channel 1 to TP101 (Y BLK VIDEO). Connect oscilloscope Channel 2 to TP97 (YA VIDC).
4. Leading edge of H syncs should be coincident ±5 ns at the 50 points. If not, move DL 11 jumpers to set proper delay.

SECTION 15

AUDIO SWITCHER PWA

15-1 INTRODUCTION

The Audio Switcher PWA (P/N 1445924) is an internal audio switcher option for ACE 25, which provides two channels of high-quality audio output, plus monitoring outputs. This PWA plugs into the switcher backplane, with four 64-pin connectors providing power and signal connections. External input and output connections are located on the lower rear panel of the Edit Controller unit. An extension board is available for test and adjustment procedures. Figure 15-1 shows the Audio Switcher PWA and identifies test points, fuse, and adjustment points.

The audio switcher handles six inputs on each channel, plus an internal silence ("Black") and a 1-kHz internal tone. A built-in, three-band equalizer (100 Hz/1 kHz/10 kHz) and a dual peak/average meter display are provided for each channel.

15-2 THEORY OF OPERATION

The following paragraphs describe general theory of operation for the Audio Switcher PWA, and its primary circuits. Figure 15-2 is a block diagram showing the main audio signal paths of the Audio Switcher PWA.

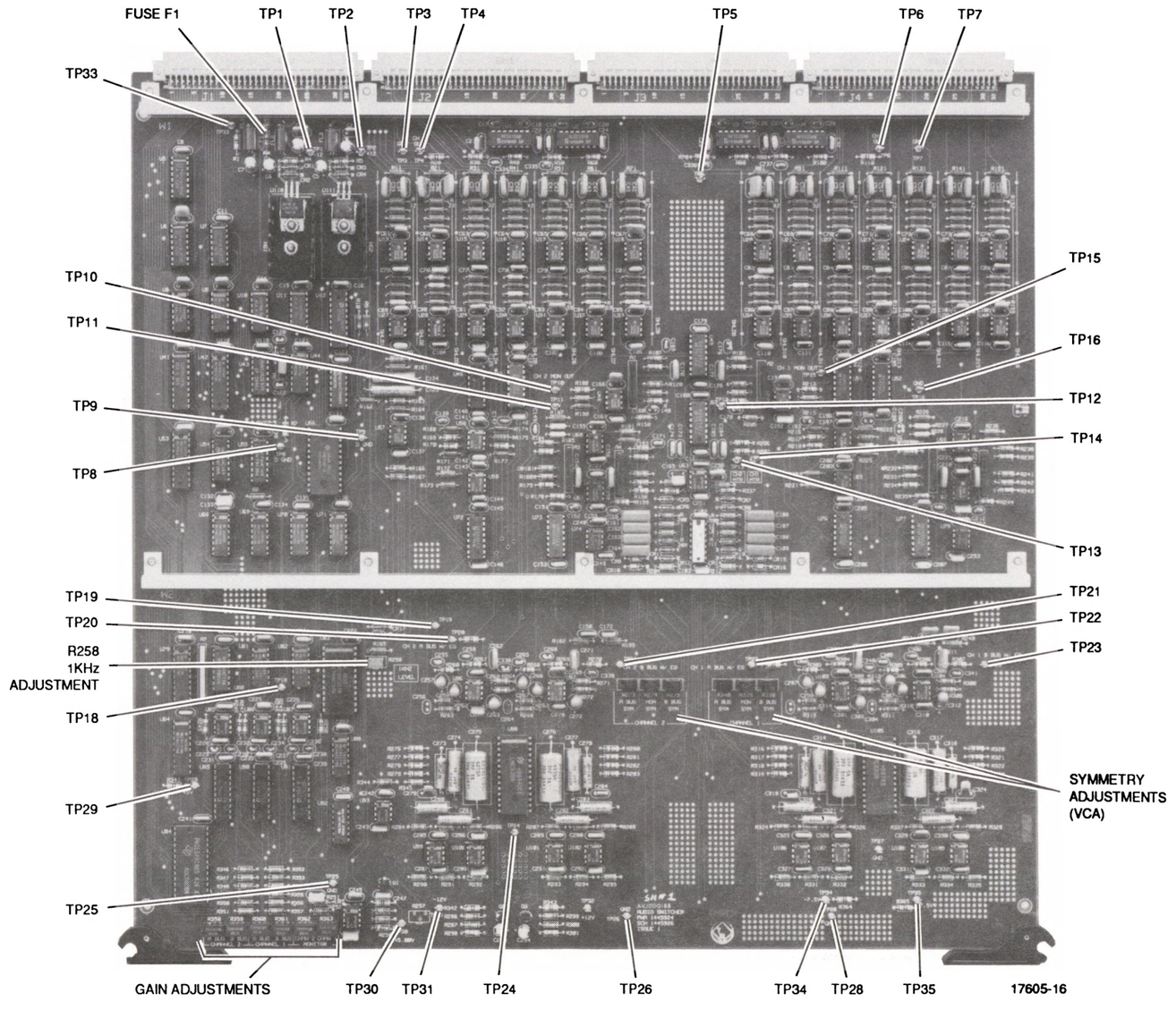


Figure 15-1.
Audio Switcher PWA

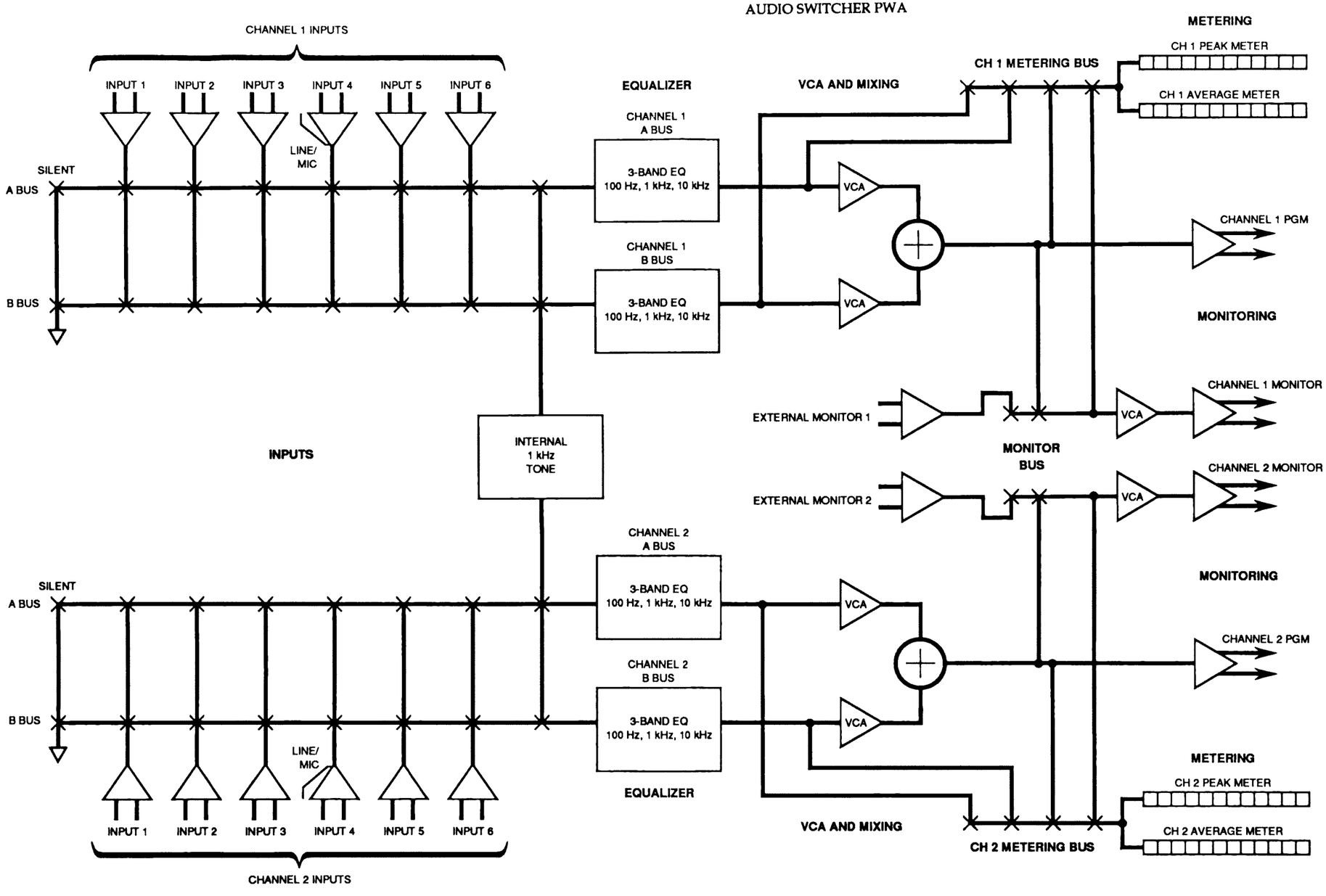


Figure 15-2.
Audio Switcher PWA Audio Signal Flow Diagram

15-3 General Description

The Audio Switcher PWA has five distinct functional areas:

- Audio Inputs (external and internal)
- EQ (Equalization) Stage
- VCA and Mixing Stage
- Metering
- Monitoring

Inputs are organized into two crosspoint buses (A bus and B bus) for each channel. The six external inputs for each channel are brought in as differential signals from external connectors, and converted to single-ended signals. Input 4 for each channel is selectable between line and microphone, with two levels (+60 dB and +40 dB) of gain for microphone input. The silent inputs ("Black") consist of four grounded crosspoint sources, while the internal 1 kHz tone is distributed to four other crosspoints. Signals on these crosspoints are selected by the operator and pass into the EQ circuitry.

Each of the four buses (Channel 1-A, Channel 1-B, Channel 2-A, and Channel 2-B) goes to a three-band equalization (EQ) stage. Levels for each band are adjustable at ±12 dB in 1 dB steps. The EQ stage permits the operator to shape the sounds differently to compensate for varying inputs on each crosspoint bus.

The main signal path for each bus continues into voice-coil amplifiers (VCAs) which control gain levels, then to mixers. The mixing stage combines the A bus and B bus for each channel into a single program output. The signals pass through output drivers and are converted back into differential signals for final output at the connectors on the rear panel.

Each channel has meter displays for peak and average on the ACE 25 data monitor. The operator selects the signals to be metered, from the metering crosspoint bus. After the EQ stage, signals from the A bus and B bus for each channel are routed to the respective metering bus. The mixed signal for each channel is also routed to the bus, plus a signal from the external monitor for that channel. It should be noted that whichever signal is selected for metering on one channel will also be selected for metering on the other channel.

Monitoring circuitry select between the external monitor inputs and the internal monitor inputs, and control the gain levels of the VCAs. A crosspoint system permits the operator to monitor the external source, or the internal mix, for each channel. The monitoring output passes through the VCA stage into an output driver, where it is converted to a differential signal for output at the monitor connector.

15-4 Power

Power input for the Audio Switcher PWA is brought in through connector J1 as +15V, –15V, +5V, +12V, and –12V. The +15V and –15V is re-regulated on this board to produce +12V and –12V. TP2 and TP32 are used to check the +12V, while TP1 and TP31 are used to check the –12V. The +5V passes through a fuse (F1), and can be checked at TP30 and TP29. The +12V is used to develop +7.5V power through Q3, showing at TP35, while the –12V is used to produce –7.5V through Q2, showing at TP34. The ±7.5V current is used to power the EQ chips, and has a five percent variability. A precision +5.00V is also developed (deviation 0.02V) through Q1, LQ1009, U95A, and U95B, and can be checked at TP30. A –5.00V is also produced, but does not appear at a test point. The analog ground has numerous test points: TP3, TP5, TP7, TP11, TP12, TP16, TP19, TP24, TP25, TP26, TP27, and TP28, and is linked to the system through connector J1 of the Dumpster bus. The digital ground also is linked through connector J1, and has three test points: TP8, TP9, and TP18. The analog and digital grounds are kept within 0.7V difference with diodes CR17 and CR18 on this PWA.

15-5 Dumpster Bus Connections

As mentioned earlier, power is supplied through the J1 connector. Address and data pairs, plus control signals, also are transferred through the J1 connector. For more information on the Dumpster bus, refer to the description of the Dumpster Bus Interface PWA (Section 11). The address, data, and control lines are buffered with U5, U6, and U7, and passed to the Dumpster bus on this PWA. The data lines are bi-directional, and are pulled off before and after the buffer.

15-6 Address/Data Information

The first digit major address decode is done by U80, with the second digit minor address decode performed by U83. The address locations are used to select crosspoints, EQ updates, and so forth. Data latch U79 is enabled by the major address 3X from U80, and is used to transfer status data back to the main CPU via the unbuffered data lines and Dumpster bus. Major address 4X, on pin 7 of U80, is the A-D output enable, which sends the analog-to-digital conversion results back to the Dumpster bus. U84 is a miscellaneous latch linked to U83, and handles items such as meter select, monitor select, line or microphone select, and high/low gain.

Data lines from the Dumpster bus are controlled by the Read/Write Not and Strobe control signals. Data from the Audio Switcher PWA to the main CPU is placed on the unbuffered lines. Data from the main CPU is buffered first then put on the local data bus on this PWA, as BD0-BD7. The miscellaneous control latch (U84) is loaded from the data bus. The EQ Update data is loaded into latch U53 and RAM 56 when the latch and memory are enabled. Data is also loaded into the A-D Select ICs (U89, U91, U92), and the crosspoint select circuitry.

15-7 EQ Update Circuitry

EQ boost/cut data is written directly from the Dumpster bus into RAM U56 when latches U41 and U53 are enabled. The EQ data is converted from the parallel to serial format, to produce an 8-bit word, with three words needed for each EQ function. A total of 24 bytes are needed by the EQ chips. After the RAM is loaded, the EQ UPDATE signal from U79 disables U41 and U53, and enables U42 to load addressing locations into U56. U55 and U54 are shift registers which transfer EQ information from RAM to the EQ chips, with PAL U12 acting as a controller and U11 as a

counter, in a series of cycles. When a cycle is completed, the counter is reset, U42 cleared, and data transfer resumed.

15-8 Line and Microphone Switching

The standard line inputs come in through the Dumpster bus (10k ohm impedance), pass through a resistor-divider network and are single-ended before going on to the crosspoint circuitry. Input line 4 for each channel is handled slightly differently. In the microphone mode, the input is switched into an amplifier section, where the 40 dB or 60 dB gain is selected. The output is then routed to the crosspoint circuitry. This switching is performed internally under software control.

15-9 Crosspoints

The crosspoint slopes and setup information (from U83) is loaded into a set of four flip-flop latches (U68, U69, U70 , U71). An R-C time constant sets all crosspoints to silent at power-up to avoid pops. Latch information is transferred to the crosspoints (U76, U77, U72, U73). Each crosspoint selects one of the eight input lines for its output.

A band-pass filter produces 1-kHz sine waves which are buffered and sent to all four crosspoints. An adjustment at R258 sets the level at exactly 0 dB. The total harmonic distortion (THD) is about 1.7 percent at this point.

15-10 EQ Circuitry

The output of the four primary crosspoints enters the EQ circuitry, which controls the amount of boost or cut in the three EQ bands. Each EQ band is handled by a gyrator, which simulates a tuned inductance. For channel 1, the digital information from the EQ Update circuitry enters EQ chip 105, where a variable resistive ladder is created, determining the amount of boost or cut for each EQ band. TP22 shows the Channel 1 A bus output after equalization, and TP23 shows the B bus output. For Channel 2, U98 is the EQ chip; TP20 is the A bus output, and TP21 is the B bus output. After leaving the EQ chips, the outputs are ac-coupled and pass on to the VCA stage.

15-11 Gain Control

Three dual DACs (U89, U91, U93) are used to develop gain control voltages for the VCAs. These DACs are set up sequentially to arrange the A bus and B bus for each channel on the same DAC. Chip select U92, together with buffered address 0, is used to determine the A-D select. The reference voltage for the DACs comes from the precision –5.00V, buffered through U93 to produce –.6V. The output of the DACs is fed into op-amps, and inverted to +.6V. A voltage divider network and adjustment sets the gain for each channel bus. The gain adjustments (R358-R363) provide a range from +.55 to –23.6 mV, with negative voltage resulting in positive gain.

Next, an RC time-constant is used to slow transitions to 15 ms to avoid audio pops. The signals pass through buffers and on to the VCA section.

15-12 Metering

Meter selection is done through differential switch U62, using decoded data from latch U84. TP14 shows the Channel 1 signal, and TP13 shows the Channel 2 signal. The audio levels go through U62, and are split for each channel into average and peak signals for meter conversion. A precision rectifier network is used to produce analog metering information for each input signal. U81/U82 are used to select the signal for conversion which goes into the analog-digital converter (U94). The A-D conversion output goes onto the unbuffered data lines and is sent through the Dumpster bus to the main CPU, where it is processed and displayed.

15-13 VCA Stage, Mixing and Final Output

The VCA stage controls the amount of gain in the signals that go into the mixing and output stages, using DBX2150 chips. The Channel 1 A bus signal with EQ is brought into the VCA (A5), and also sent to the metering stage. The VCA converts the voltage input into current output. The control signal comes from the Gain Control circuitry, and is fed into the VCA; positive voltage produces attenuation, and negative voltage results in gain. The Channel 1 A bus symmetry is adjusted with R340, to minimize THD. A typical specification for THD is 0.1 percent. The output of the VCA is converted from current back into voltage, and routed into U66. U66 performs the mixing by summing the A bus and B bus inputs, and also produces a gain of 1.77, to boost the signal. The mixed output signal can be checked at TP6. The Channel 2 A bus and B bus goes through similar gain and mixing, with the output mix signal appearing at TP4.

The Channel 1 mixed output from U66 goes into audio driver U4, which has two sides. U4B is used to drive the positive side out, while U4A drives the negative side, which is derived from the inverted signal. Together, U4A and U4B are capable of driving 600 ohms up to +25 dB of double-ended output. U4 should not be grounded to produce a single-ended output, since this may result in over-heating. The Channel 2 output follows a similar path through U60 (mixing) and U1 (output).

The Channel 1 mixed signal is also passed through U66B to the monitoring and metering stages, and Channel 2 mix is passed through U60B. Both signals are divided down to about 0.56V for internal processing.

15-14 Monitoring

The external monitoring input enters via the Dumpster bus. It is converted into a single-ended signal (U20, U34), and sent to differential switch U49. This differential switch is controlled by decoded commands from the miscellaneous control latch (U84), and selects between the external and internal signals for monitoring. The output from U49 (for Channel 1) is ac-coupled before entering the VCA stage, which sets the output level (using R339 adjustment). This VCA is matched with the other VCAs for the program signals to produce correct audio level output. A gain stage at U50A boosts gain by a factor of 1.7, with the resulting signal displayed at TP16. Next, the monitor output signal is split, with a branch sent to the metering crosspoint network, and the primary signal entering a driver stage (U3). This driver stage produces the final output signal (600 ohms at +25 dB) for the monitor jack. Channel 2 circuitry replicates Channel 1 circuitry.

15-15 FUSES AND TEST POINTS

The following paragraphs describe the fuses and test points on the Audio Switcher PWA.

15-16 Fuses

The Audio Switcher PWA has one fuse, F1 (P/N 070-443). Fuse F1 is rated at 5.0 amp and soldered on two posts. Refer to Figure 15-1. Replace fuse with equivalent fuse.

15-17 Test Points

Table 15-1 lists the test points and their associated signals.

15-18 ADJUSTMENTS

The following paragraphs describe the test equipment and adjustments that are performed on the Audio Switcher PWA.

15-19 Test Equipment

Table 15-2 lists the recommended test equipment for performing adjustments on the Audio Switcher PWA.

15-20 Power Supply Checks.

Check the following points for the corresponding voltages. All points should have less than 50 mV of ac current.

TP1	–12V	±0.5V
TP2	+12V	±0.5V
TP30	+5.00V	±0.05V
TP33	+5V	±0.1V
TP34	–7.5V	±0.4V
TP35	+7.5V	±0.4V
U95, Pin 1	–5.00V	±0.05V

15-21 Operational Adjustments

The internal audio switcher levels are adjusted using the keyboard's rotary knob and the VU level and equalization displays on the monitor screen.

Press **HOME**, then ***AUDIO SWITCHER*** to access the Audio Switcher Function Choice menu.

The soft keys in the lower left hand corner indicate the functions that can be adjusted: INPUT LEVEL, M/E FADER, and DS FADE SILENT, EQ SETTINGS. For each adjustment, the source audio (**A, B, C, AUX1, AUX2,** or **AUX3** on the keyboard) and the channel (***CHANNEL 1, CHANNEL 2,*** or ***BOTH CHANNELS***) to be adjusted must be selected.

Table 15-1. Audio Switcher PWA Test Points

Test Point	Description
TP1	–12V
TP2	+12V
TP3	Analog Ground
TP4	Channel 2 Audio Out
TP5	Analog Ground
TP6	Channel 1 Audio Out
TP7	Analog Ground
TP8	Digital Ground
TP9	Digital Ground
TP10	Channel 2 Monitor Audio Out
TP11	Analog Ground
TP12	Analog Ground
TP13	Channel 2 Meter
TP14	Channel 1 Meter
TP15	Channel 1 Monitor Audio Out
TP16	Analog Ground
TP17	NOT USED
TP18	Digital Ground
TP19	Analog Ground
TP20	Channel 2 A Bus Audio with EQ
TP21	Channel 2 B Bus Audio with EQ
TP22	Channel 1 A Bus Audio with EQ
TP23	Channel 1 B Bus Audio with EQ
TP24	Analog Ground
TP25	Analog Ground
TP26	Analog Ground
TP27	Analog Ground
TP28	Analog Ground
TP29	+5V
TP30	+5.00V (precision voltage)
TP31	–12V
TP32	+12V
TP33	+5V
TP34	–7.5V (5 range)
TP35	+7.5V (5 range)

Table 15-2. Recommended Test Equipment

Equipment	Recommended Model or Type
Oscilloscope	Tektronix 465A
Probe, Oscilloscope (2)	Tektronix 6106
Digital Multimeter	Fluke
Audio Signal Generator	Sound Technology 1710
Cable, Coax (10)	XLR Female to Mini XLR Male
Cable, Coax (6)	XLR Male to Mini XLR Female

15-22 Audio Source Input Level Adjustment

Adjust the audio input level to internal audio switcher as follows:

1. Verify that all system audio cables are properly connected from source VTRs and other machines to the ACE 25 rear panel and record VTR.
2. Press *INPUT LEVEL* on Audio Switcher Function menu. The VU meter window appears in the upper right corner of the menu display.
3. Select the audio source to be adjusted (**A, B, C, AUX1, AUX2,** or **AUX3**). The audio source selected is displayed at the top of the VU meter window.
4. Select the audio channel on which to set input levels (**CHAN1/CHAN2** or **BOTH CHANNELS**). The audio channel selected is displayed at the top of the VU meter window, and is highlighted.
5. If the source is recorded with Bars and Tone at the head, rewind tape to beginning and put VTR into **PLAY**.
6. Set output playback level of recorded tone on source VTR to 0 dB or 100 VU.
7. Turn rotary knob on keyboard clockwise to increase audio input level; counterclockwise to decrease level. Observe level displayed on the VU meters on screen, and adjust for 0 dB. In this way, input level to ACE 25 matches output level from source VTR. Check also that 0 dB or 100 VU reads on the record VTR's input meters.
8. Follow the same procedure for all channels on all other sources used, both VTR and AUX sources. Repeat steps number 3 through 7 as required. Adjust input audio levels as required; however, it is recommended that VTR and source playback levels remain set at 0 dB or 100 VU.
9. Press *HIDE VU* to remove the VU display from the screen.
10. Press *RETURN* to return to previous soft key menu.

15-23 Audio Monitor Level Adjustments

Adjust audio monitor levels by pressing *MONITOR LEVEL* on the Audio Switcher Function menu. Then follow steps number 2 through 7 as outlined above for input level.

15-24 Equalization Adjustment

The following procedure is used to perform Equalization Adjustment:

1. Adjust equalization of audio output from the internal switcher by pressing *EQ SETTING* on the Audio Switcher Function menu.

2. Select audio source to be adjusted (**A, B, C, AUX1, AUX2,** or **AUX3**).

3. Press soft key to select low, mid or high audio frequency range to be equalized. The EQ window appears in the upper right of the menu display, showing bar graphs for each EQ range. The selected range is highlighted.

4. Select the audio channel to equalize (CHAN1/CHAN2 or *BOTH CHANNELS)*. Selected audio channel and source are displayed at the top of the EQ window.

5. Each EQ range is marked off in 1 dB steps, from +12 to –12, with a small solid white bar marking the current EQ setting. Turn the rotary knob clockwise to increase the EQ level, counterclockwise to decrease the EQ level. With the VTR or AUX source in **PLAY**, observe the marker as displayed on the bar graph, and adjust for the desired audio signal equalization.

6. Follow the same procedure for all channels on all other sources used in the edit session. Repeat steps number 2 through 5 as required.

15-25 1-kHz Level Adjustment

Adjust R258 to set the 1 kHz tone level to 0 dB. Check TP20, TP21, TP22, and TP23 for minimum total harmonic distortion (THD). The Audio Switcher PWA should be placed on the extender board for this adjustment.

15-26 Symmetry Adjustments

The six symmetry adjustments listed below are used to correct control voltages to their associated VCAs to minimize THD, and should be performed prior to gain adjustments, utilizing the extender board.

- R273 Channel 2 A Bus Symmetry
- R274 Channel 2 Monitor Symmetry
- R275 Channel 2 B Bus Symmetry
- R338 Channel 1 B Bus Symmetry
- R339 Channel 1 Monitor Symmetry
- R340 Channel 1 A Bus Symmetry

15-27 Gain Adjustments

The Audio Switcher PWA can be run at unity gain, or with a maximum of +40 dB flat gain. The EQ stages can add up to +12 dB across the three bands; the VCAs can add +4 dB gain. If the PWA is set up as a unity system, the control voltages to the VCAs should be very close to 0 if the channels are active, and +0.56V if the channels are off. If the board is run at +4 dB gain, the control voltages to the VCAs will be approximately –0.23 mV.

The gain adjustments are listed below:

- R358 Channel 2 A Bus
- R359 Channel 2 B Bus
- R360 Channel 1 A Bus
- R361 Channel 1 B Bus
- R362 Channel 2 Monitor
- R363 Channel 1 Monitor

SECTION 16

KEYBOARD AND DATA MONITOR

16-1 INTRODUCTION

This section covers service procedures for the ACE 25 Keyboard and the ACE 25 Desktop Display Monitor.

16-2 ACE 25 KEYBOARD

The following paragraphs describe the ACE 25 Keyboard and cover procedures for changing voltage type, and replacement of major sub-assemblies.

16-3 General Description

Figure 16-1 shows top and bottom views of the ACE 25 Keyboard (P/N 1431701). Access to internal components of the ACE 25 Keyboard is gained by removing the six screws securing the bottom section of the plastic case.

The rear panel of the ACE 25 keyboard (shown in Figure 16-2) contains the ON/OFF switch, RS-422 cable connection to the Edit Controller, and the connection for an optional comments keyboard.

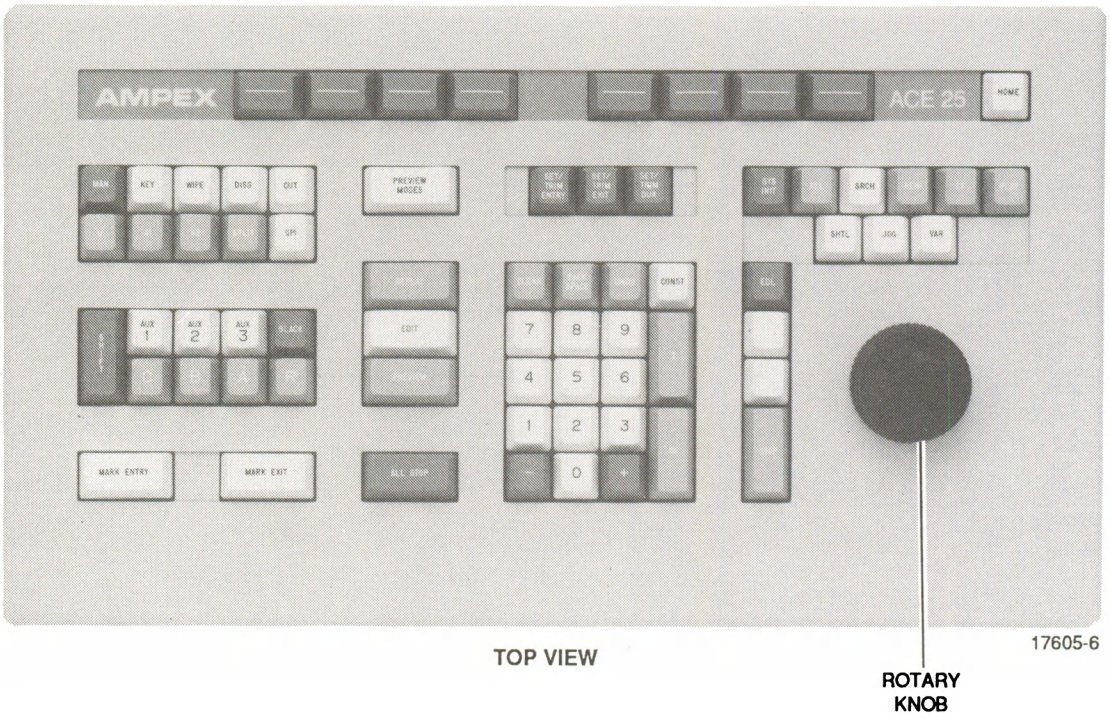


Figure 16-1. ACE 25 Keyboard

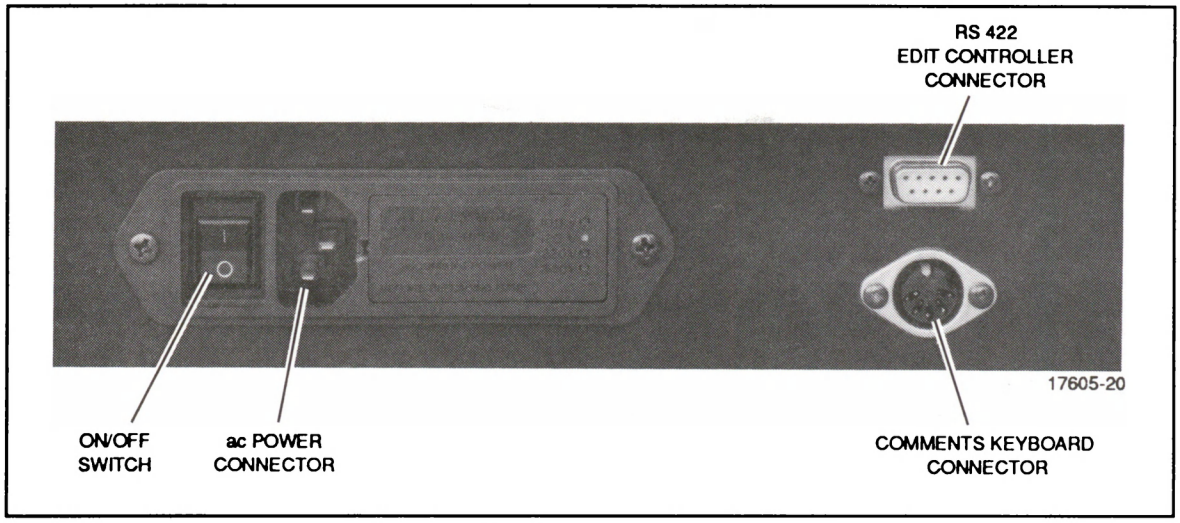


Figure 16-2. Keyboard Rear Panel

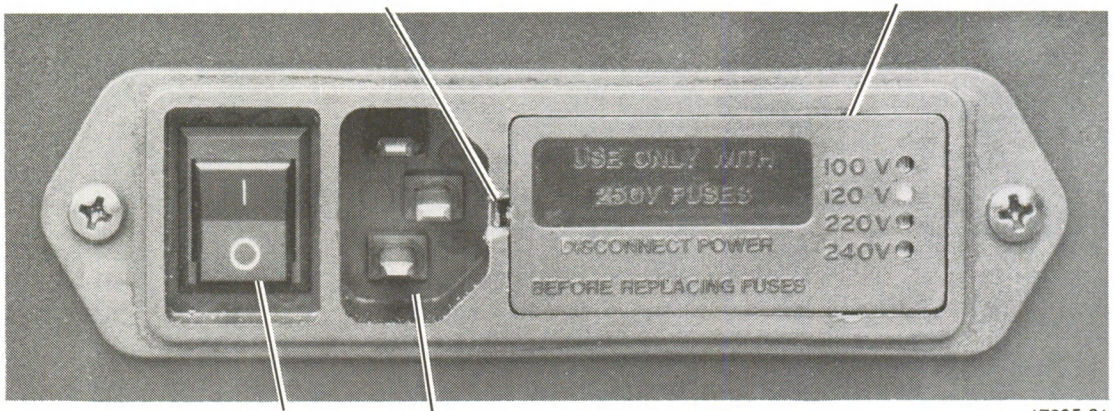
16-4 Keyboard Line Voltage Selection

Check keyboard to verify that it is set up for the line voltage used at the installation site. Keyboard is capable of accepting 120V or 240V power. Figure 16-3 shows the fuse holder and voltage changeover circuit board. The small voltage changeover circuit board inserted in slot behind fuse holder assembly on the keyboard rear panel determines appropriate voltage to be applied to keyboard. The changeover circuit board has a white plastic stem that protrudes through one of four holes in the fuse holder assembly cover, indicating voltage setting. Holes are marked 100V, 120V, 220V, and 240V, but only 120V and 240V positions are used. At sites using 120V, tip of white plastic stem should appear in the hole marked 120V. At sites using 240V, stem should appear in the hole marked 240V.

To change the changeover circuit board for site voltage, proceed as follows:

1. Unplug power cord at keyboard rear panel.
2. Insert small flat blade screwdriver into slot provided in fuse holder assembly and pry assembly from the keyboard unit. Refer to Figure 16-3.
3. Use needle nose pliers to remove changeover circuit board from the keyboard unit.
4. Position changeover circuit board so that correct line voltage is visible (120V or 240V) on outer edge of board. Place white plastic stem to outer edge of board.
5. Reinstall changeover circuit board into keyboard.
6. Install correct fuse into fuse holder. Use 1A, slow blow fuse with 120V, and 0.5A, slow-blow fuse with 240V.
7. Reinstall fuse holder into keyboard.
8. Check that white plastic stem protrudes through hole in fuse assembly cover marked with appropriate voltage.

FUSE HOLDER ASSEMBLY



VOLTAGE CHANGEOVER CIRCUIT BOARD

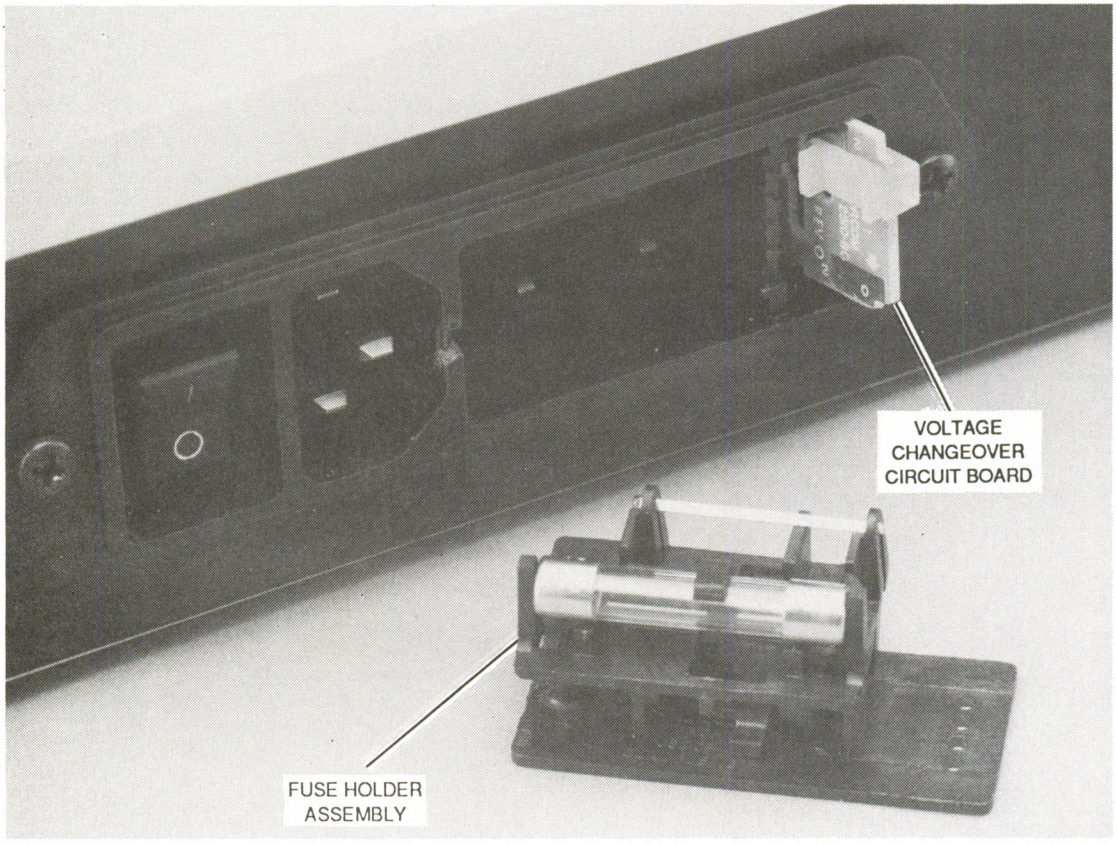


Figure 16-3. Keyboard Voltage Selection

16-5 Keyboard Knob Adjustment and Replacement

The control knob assembly on the ACE 25 can be adjusted to increase or decrease turning resistance. Figure 16-4 shows the various pieces of the knob assembly. Remove the plastic cap to reveal the nut securing the outside knob. Use a pair of needle-nose pliers to adjust resistance to desired amount. Replace plastic cape.

To replace entire knob assembly:

1. Power off keyboard and remove cables.
2. Remove plastic cap from knob to expose nut.
3. Remove nut with needle-nose pliers.
4. Remove outside knob.
5. Remove bushing on shaft.
6. Turn keyboard over and remove 6 screws securing bottom section of case. Refer to Figure 16-1. Remove bottom case section.
7. Unplug two connectors for leads from the knob assembly.
8. Turn keyboard over once more.
9. Remove 3 cross-recessed screws securing knob body to case.
10. Remove knob body.

Reverse above steps to replace knob assembly.

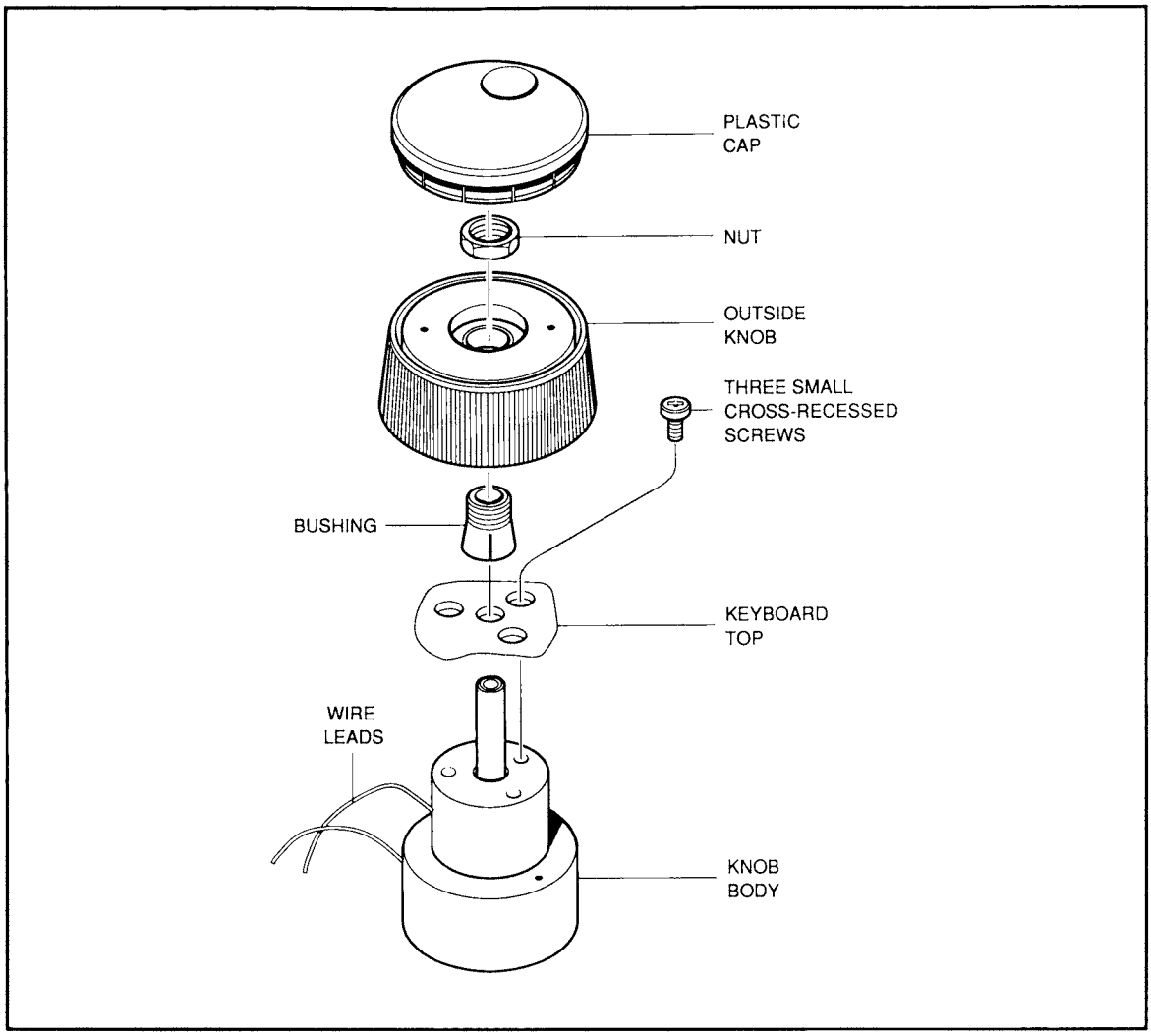


Figure 16-4. Keyboard Knob Replacement

16-6 Keyboard Power Supply

The ACE 25 keyboard contains an internal power supply which converts the ac power to dc power. This power supply has its own fuse. See Figure 16-5 for fuse location.

To replace the fuse:

1. Turn off power to keyboard and disconnect power cord and cable.
2. Turn keyboard over and remove 6 screws securing bottom section of case. Remove bottom case section.
3. Locate and remove fuse.
4. Replace fuse with equivalent (2 amps).
5. Reverse steps number 1 through 3.

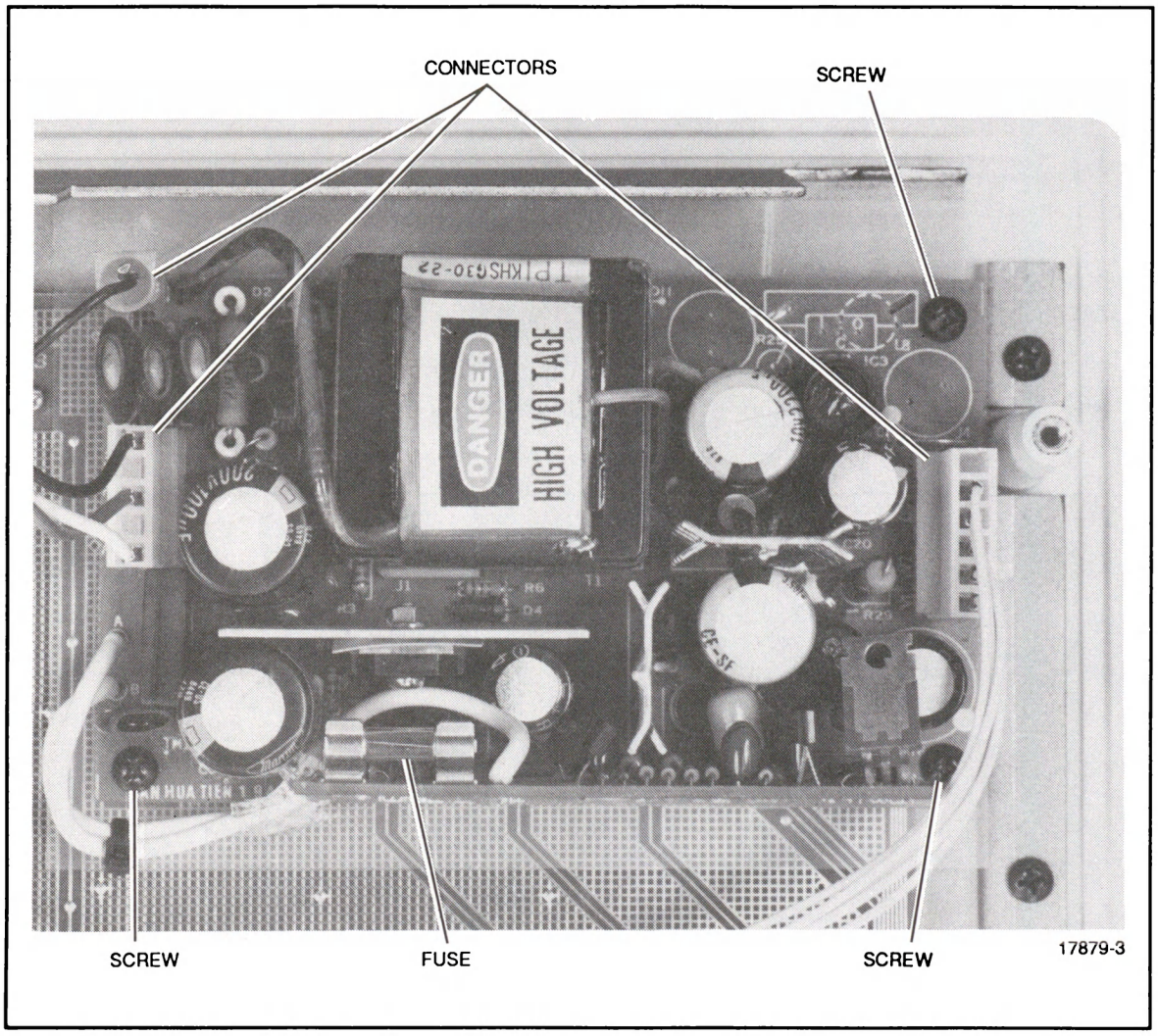


Figure 16-5. Keyboard Power Supply

To replace the power supply:

1. Turn off power to keyboard and disconnect power cord and cable.

2. Turn keyboard over and remove six screws securing bottom section of case. Remove bottom case section.

3. Carefully disconnect three connectors for leads to power supply. Excessive force may damage connector tabs.

4. Remove three cross-recessed screws securing power supply to keyboard case, and remove power supply.

To replace power supply, reverse steps number 1 through 4.

16-7 ACE 25 TABLETOP DATA MONITOR

The following paragraphs describe the Tabletop Data Monitor , including its controls and adjustments.

16-8 Description

The Tabletop Data Monitor (P/N 1430983) is a 14-inch, high-resolution, monochrome monitor with detachable base. Figure 16-6 shows front and rear views of the monitor. The built-in power supply can be used with 95-135 Vac or 190-270 Vac by changing the power jumper. Figure 16-7 is a functional block diagram of the data monitor.

An RS-422 cable connects the monitor to the Edit Controller, enabling monitor to receive video signals developed on the Monochrome Video Display PWA. Table 16-1 identifies these video connector signals.

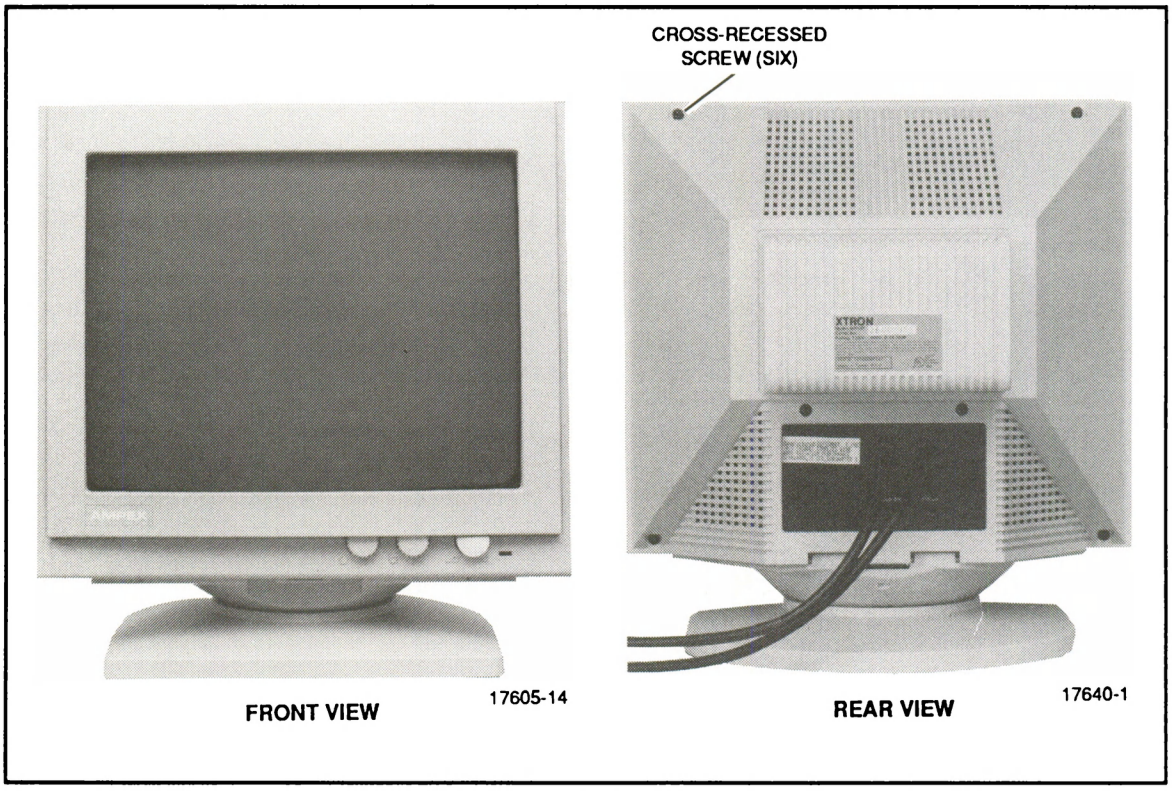


Figure 16-6. Data Monitor

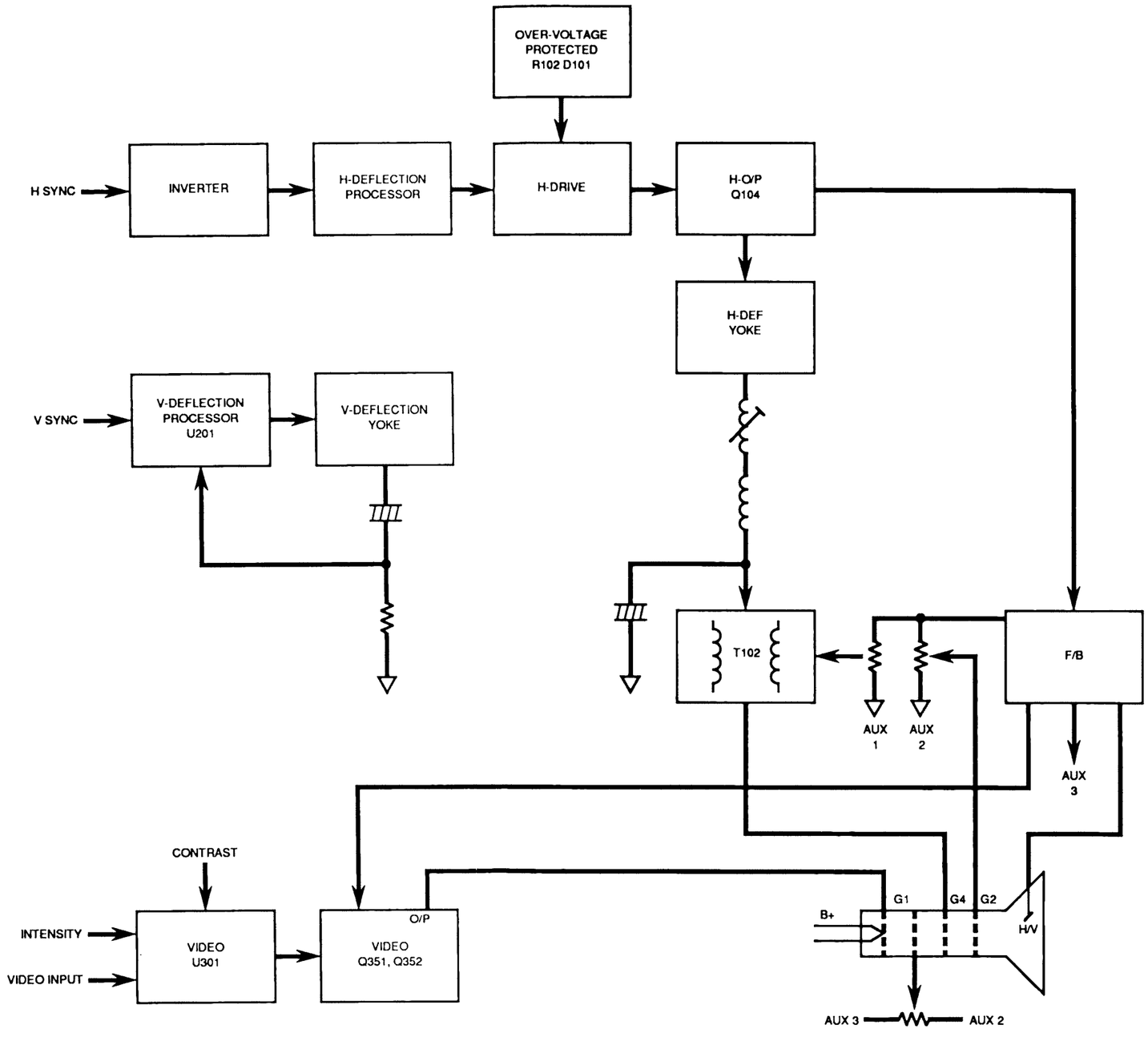
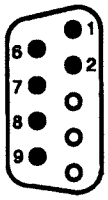


Figure 16-7.
Data Monitor Functional Block Diagram

Table 16-1. Data Monitor Connector Signals



Pin No.	Signal	Pin No.	Signal
1	Ground	7	Video
2	Ground	8	Horizontal
6	Intensity	9	Vertical

16-9 External Monitor Controls and Adjustments

The exterior monitor controls are located on the front and rear of the monitor. Table 16-2 identifies these controls and their functions.

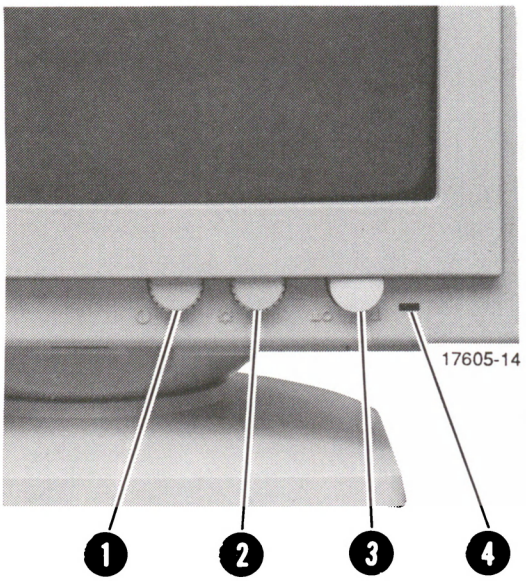
16-10 Internal Monitor Controls and Adjustments

The data monitor must be opened to change interior controls and adjustments. To access internal monitor controls and adjustments:

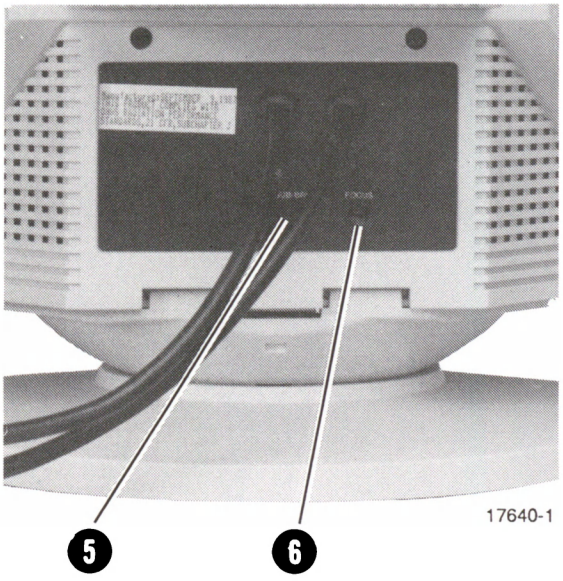
1. Power off the monitor and unplug power and video cables.
2. Remove six cross-recessed screws securing rear cover (refer to Figure 16-6).
3. Carefully pull rear cover off, feeding power and video cables through hole.
4. Remove two cross-recessed screws securing electronic chassis assembly to front case section (see Figure 16-8).
5. Carefully turn electronic chassis to access component side.

Table 16-3 shows the location of interior controls and adjustments. Figure 16-9 shows the location of the voltage selection jacks. There may be slight differences among monitors due to production changes. On some monitors, a wire may be used for voltage selection in place of jumper jacks; on other monitors, the size controls may be located in different positions.

Table 16-2. Data Monitor External Controls and Adjustments



FRONT ADJUSTMENT CONTROLS



REAR ADJUSTMENT CONTROLS

Index No.	Control	Description
1	Contrast	Sets contrast between normal and high-lighted video.
2	Brightness	Sets intensity of video display.
3	ON/OFF	Push-in contact switch turns monitor on or off when pushed. The LED next to switch is lit when power is on.
4	Power-On LED	Lights when power is on.
5	Sub-Brightness (Sub-Bri)	Sets background luminance level.
6	Focus	Increases or decreases focus (sharpness) of characters on screen.

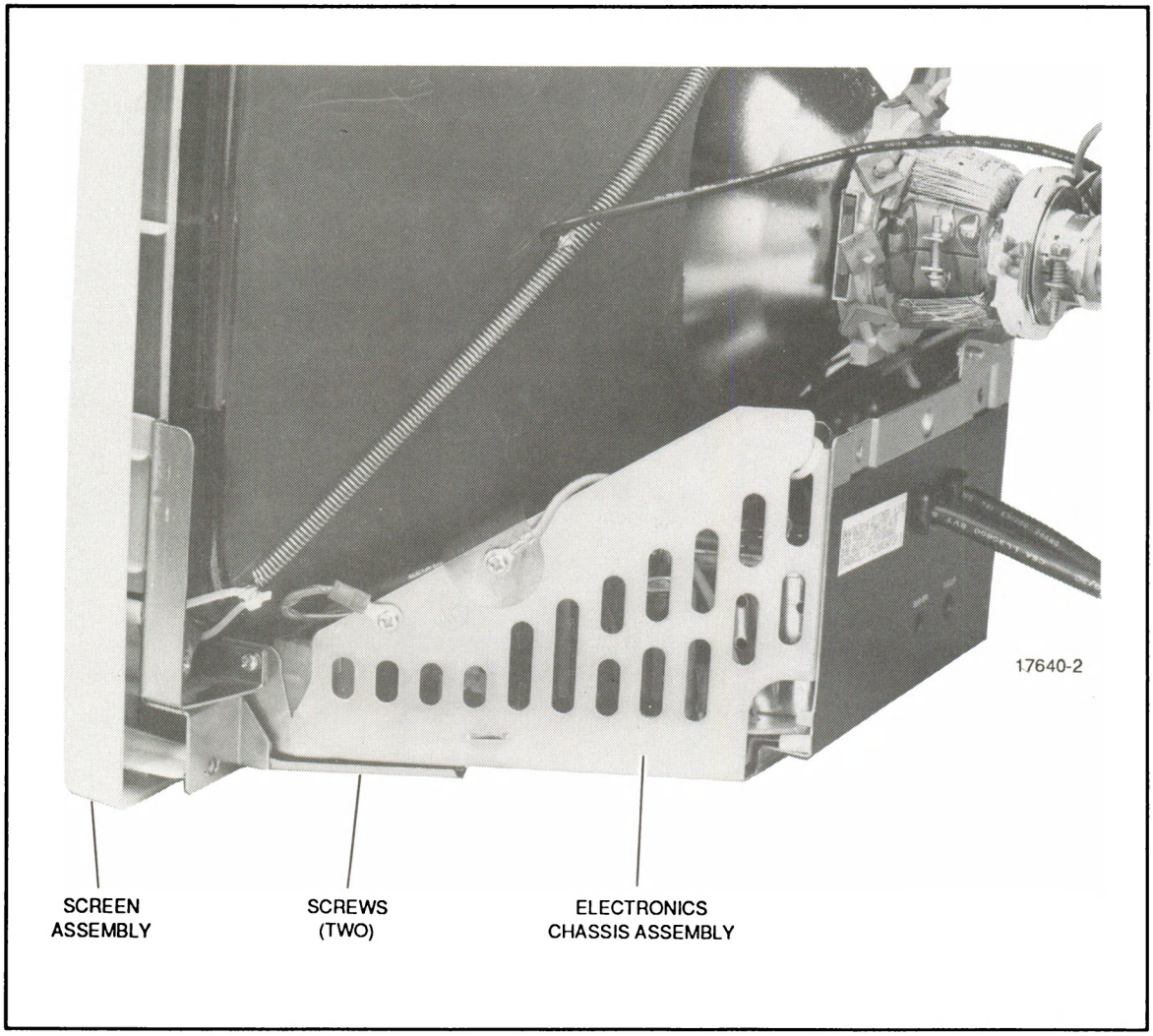
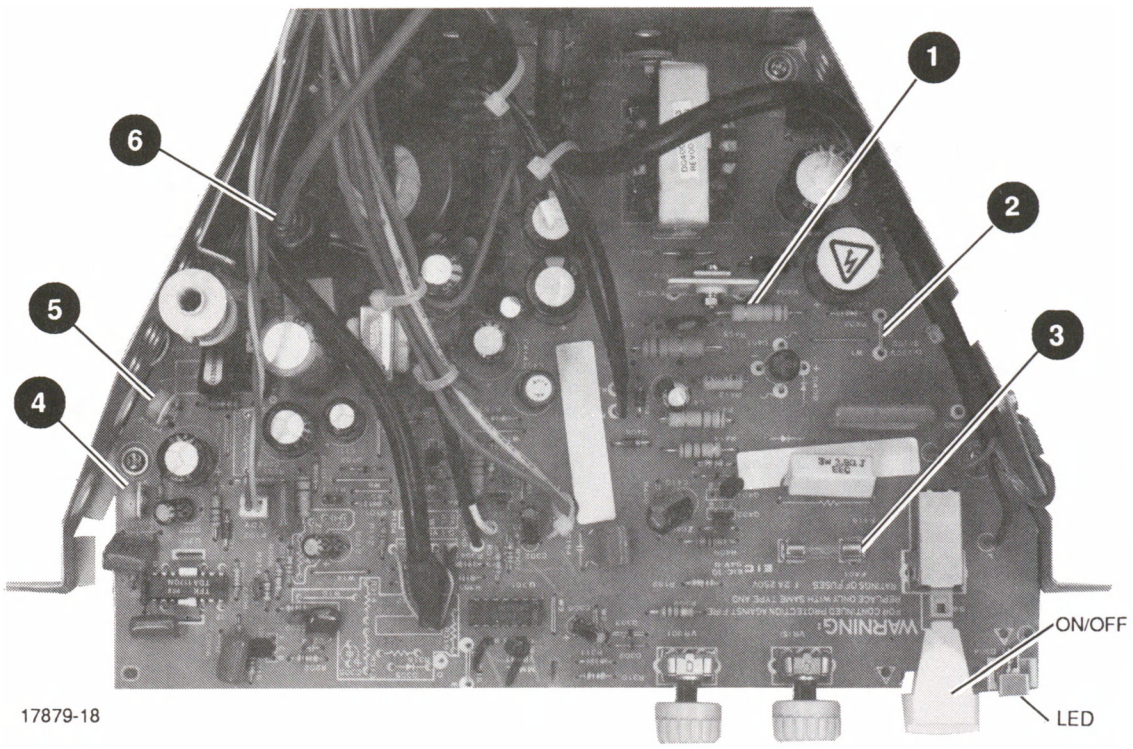
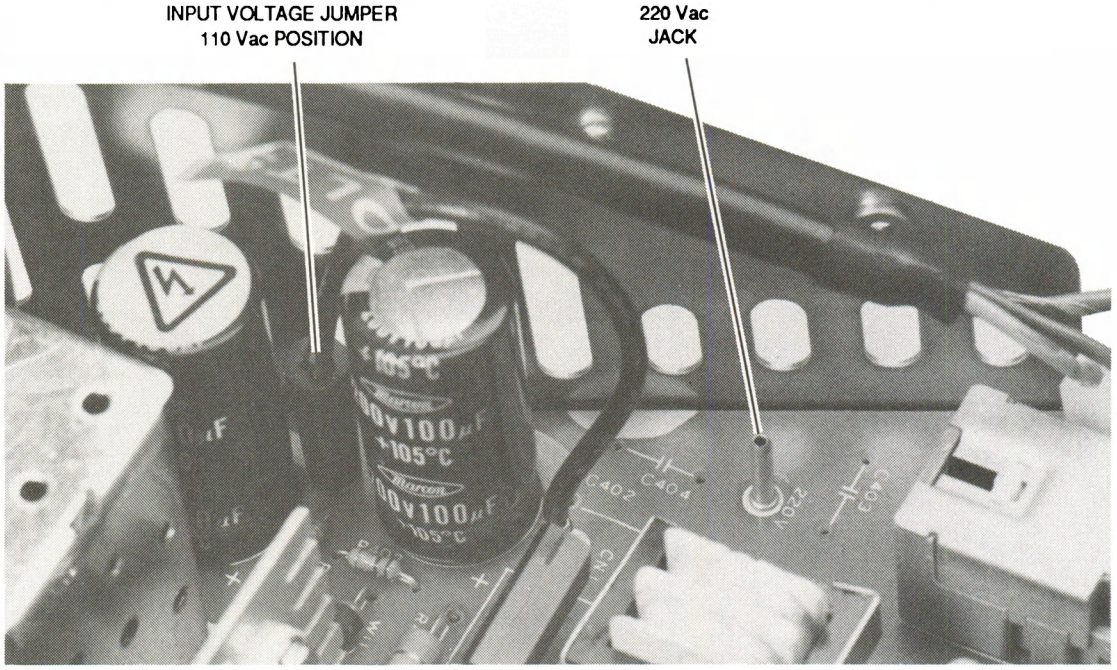


Figure 16-8. Data Monitor Electronics Chassis

Table 16-3. Data Monitor Internal Controls and Adjustments

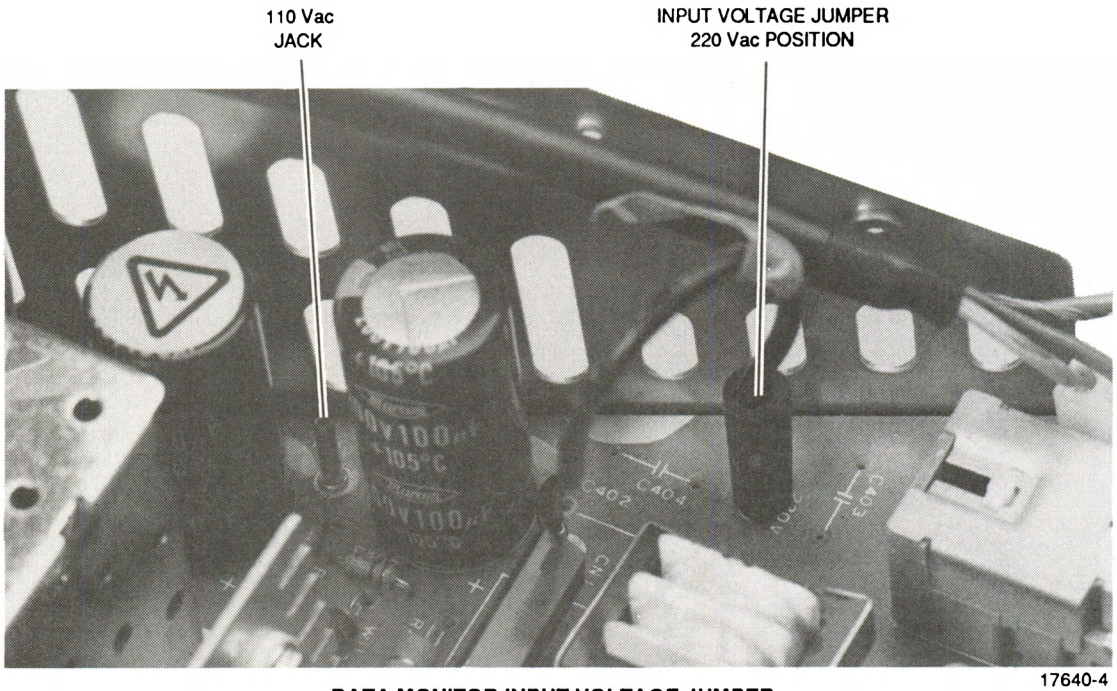


Index No.	Control	Description
1	110 Vac Jack or Jumper	Selects 110 Vac input voltage.
2	220 Vac Jack or Jumper	Selects 220 Vac input voltage.
3	Fuse	Short 2 amp fuse, identical for 110 Vac or 220 Vac operation.
4	VR201 (V SIZ)	Vertical size control. Clockwise movement increases size; counter-clockwise movement decreases size.
5	VR202 (V LIN)	Vertical linearity control. Controls vertical spacing of displayed character. To adjust, display hatch pattern or character "0" over whole screen. Vertical spacing should be same at top, bottom, and center of screen.
6	L101	Horizontal size control. Core of L101 controls horizontal size; a small plastic screw driver is used to make adjustments. Clockwise movement increases size; counter-clockwise movement decreases size.



17640-3

DATA MONITOR INPUT VOLTAGE JUMPER
110 Vac POSITION



17640-4

DATA MONITOR INPUT VOLTAGE JUMPER
220 Vac POSITION

Figure 16-9. Data Monitor Voltage Selection

APPENDIX A

ERROR MESSAGES

A-1 GENERAL INFORMATION

ACE 25 has a software-based error detection and reporting system. Each error condition is identified by a unique error code and message. An error log records an error and remembers the last 20 keystrokes preceding the error. This error log can be viewed later to analyze possible causes of error.

The error detection and reporting system entails four sequential stages:

- **Error Generation.** When software process detects an error condition, software macro procedures generate an error status block, containing error code, error format string, and parameters needed to construct error message.
- **Error Propagation.** Error codes are transferred through function calls to other software processes, and an error code response is returned to the software process that generated or detected the initial error condition.
- **Error Resolution.** When error code reaches software process that can correct error condition, error condition is cleared.
- **Error Reporting.** Error message is displayed to operator, using error code, error format string, and error parameters. Error log is updated with latest error information.

Error messages are displayed at the top of the data monitor screen. Table A-1 lists in numerical order the error messages which appear most frequently; and Table A-2 lists all error messages, according to code number and type.

A-2 ERROR LOG

The error log is designed to assist users in identifying and correcting problems that may occur on the system. Each error code has its own discreet identification number and associated message.

To view and copy the error log perform the following procedure:

1. Connect any Centronics parallel printer, IBM compatible, to the ACE 25 parallel printer port, located on the rear panel of the edit controller chassis.

2. To view the error log, press the following keys on the ACE 25 keyboard:
   - **SYS INIT** key
   - ***MORE*** soft key
   - ***SHOW HISTORY*** soft key
3. To print the error log, press ***PRINT HISTORY*** soft key.

Note

If printer is not available, copy on-screen Error History and Command History on paper by hand.

If Ampex Technical support is needed for hardware and software solutions, a copy of the error log can be helpful in resolving problems. To send a copy of the error log to Ampex, use the following numbers:

- Ampex fax number: (415) 367-2551
- Technical support direct telephone number: (415) 367-3807

A-3 CRASH SYSTEM

If a system crash occurs, the source of the crash can be identified. In the event of a system crash, the editing session stops and the following information appears on the screen:

FATAL SYSTEM ERROR

PLEASE REPORT ERROR CODES

***E=XXXX	P=XXXX	A=XXXX-XXX
***X=XXXX	Y=XXXX	Z=XXXX-XXXX

Copy information from screen and send it, together with a copy of the error log, to Ampex Technical Support.

Table A-1. Common Error Codes

Code No.	Error Message or Meaning
18	Color Field 1 Detector PWA interrupt failure
507	Invalid burst in system video reference
508	Locking to new color field sequence
512	Can't find device on ILC Channel 0
518	Can't find ILC Board
520	ILC Board is sick
524	Illegal message received, Channel 0
526	Input Channel 0 not ready
528	ILC Channel 0 is being re-configured
532	Output Channel 0 is not ready
534	ILC Channel 0 needs to be re-configured
1200	Communications processor busy
1202	Check sum error on Channel 0
1204	Invalid message on Channel 0
1205	Invalid response on Channel 0
1206	No response on Channel 0
1207	Channel 0 not configured
1208	Communications time-out on Channel 0
1209	UART error on Channel 0 (XX) Bits in error code interpreted as follows: Bit 7: Received Break Bit 6: Framing Error Bit 5: Parity Error Bit 4: Overrun Error Bit 3: Transmitter Empty Bit 2: Transmitter Ready Bit 1: Receiver FIFO Full Bit 0: Receiver Ready
1700	Comments Keyboard failed diagnostic test
1702	Invalid command sent to ACE 25 keyboard
1704	RAM Test failed on ACE 25 keyboard
1706	Invalid ROM on ACE 25 keyboard
1708	Stuck key on ACE 25 keyboard
4014	Dumpster memory failure; address 00, wrote 55, read 00

Table A-2. ACE 25 Error Messages

Code No.	Error Message or Meaning
General (Codes 1-99)	
1	Internal error botched boolean test
2	Bad code cksum start=%1P, length=%.4X
4	Bad index:% s =% .4X
6	Bad ixidReply: %.4X
8	Bad pointer: %4P
10	Bad process: %.4X
12	Bad state: %.4X
14	Bad service: %.4X
16	Bad type: %s = %.4X
18	Call of non function: %1P
20	Developer dump: %.4X %.4X %.4X %.4X
21	Divide trap: %4P
22	Format block unknown format
24	Reference video missing or invalid
26	Memory clobber type %d
28	Feature not implemented
30	Format string output overflow
32	Attempted deadlock in process %.4X
34	pSOS error: %d %.4X
36	Reply mismatch: services %.4X %.4X
37	Session Reset: %s
38	Stack overflow in process% d
40	Stack overflow danger in process %d. %d words remaining
42	Format string tyArg bad
44	Format string width overflow
Unallocated (Codes 100-199)	
PERR Error (Codes 200-299)	
200	Buffer size %d too small

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Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
	PFIO or MSDOS Error (Codes 300-499)
300	Cannot fit MIF/SWIF file into buffer
302	Cannot reset floppy disk system
304	Internal %s error on drive %c: [%4.4X]
306	Cannot change disk label on drive %c:
308	Cannot create disk label on drive %c:
309	No disk in drive %c:
310	Bad data written to track %d
312	Disk in drive 4c is not formatted
314	No disk in drive %c or disk is write-protected
316	Invalid argument to DOS call
322	Can't use file %s, too many files open
324	Can't access file %s
330	File% s exists already
332	Invalid handle for file %s
334	File %s not found
336	No space left for file %s
342	No such disk drive as %c
344	Not a valid character
346	Printer bios timed out. Status %2.X
348	Printer busy. Status %.2X
350	Printer halted
352	Printer not assigned
354	Printer not connected to ACE 25. Status %.2X
356	Printer out of paper. Status %.2X
358	Printer is off line. Status %.2X
360	Printer is turned off. Status %.2X
362	Printer status %.2X not recognized
354	The last item on file %s is incomplete
366	Can't send xon signal to transmitting side
368	Bad baud rate %d for serial port %d
370	Bad parity for serial port% d

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
	PFIO or MSDOS Error (Codes 300-499) [Continued]
372	Bad number of stop bits %d for serial port %d
374	Bad word length %d for serial port %d
376	Break detected during %s on serial port %d
378	Framing error during %s on serial port %d
380	Serial file transfer halted
382	Data over run during %s on serial port %d
384	Parity error during Ts on serial port %d
386	First char came on receiving
388	Timed out during %s on serial port %d
390	Unknown file transfer port
392	BIOS error code not recognized: %d on function %d
394	Disk error code not recognized: %.2X
398	MS_DOS error code not recognized: %d
400	Transfer completed
402	FUNC_XFER can't read complete item
404	FUNC_XFER can't write complete item
406	Transfer not done
408	No xon signal received for transmission
	PISP Error (Codes 500-599)
500	Found %s device on %s device ILC Channel %d
502	The MIF/SWIF file size is too big
504	Channel %d already booting
506	This device doesn't need to boot
507	Invalid burst in system video reference
508	Locking to new color field sequence
510	Can't exchange msgs. Not in ILC_CONFIG
512	Can't find device on ILC Channel %d
514	Output channel %d not clear on config
516	Previous Communication Error
518	Can't find ILC Board

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
	PISP Error (Codes 500-599) [Continued]
520	ILC Board is sick
522	ILC %d buffer overflow
524	Illegal message received on channel %d
526	Input channel %d not ready
530	Attempt to send null msg on channel %d
532	Output channel %d not ready
533	Ring spline error on channel %d
534	ILC Channel %d needs to be re-configured
536	Invalid Communication Type
537	Interrupt process out of error blocks
542	Invalid Quatro keyboard message
544	Bad raw key code %.2X %.2X
546	Raw key eaten
	Unallocated (Codes 600-699)
	PWIN or Vitamin C Error (Codes 700-899)
700	Window cannot hide: %.4X
702	Window cannot move: %.4X
704	Window cannot select: %.4X
706	Window cannot show: %.4X
708	Internal error
710	No control data for EQ Meter
712	Window not currently active: %.4X
	Timecode Error (Codes 900-999)
900	Bad TC Standard
906	TcCMP Failed: %.4X
908	Drop Frame Error [%.11t]

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
Timecode Error (Codes 900-999)	
910	Drop Frame Not Allowed In PAL
912	Drop Frame Not Allowed in PAL [%.11t]
913	Timecode discontinuity on transport %c
914	Division of zero by zero
916	Division by zero
918	First Timecode Is Undefined [%.11t]
920	Invalid BCD Digit [%.11t]
922	Invalid TC Number [%.11t]
926	Drop Frame and Non-Drop Frame Mixed
930	Second Timecode Is Undefined [%.11t]
932	Edit speed overflow
934	Edit speed underflow
936	Timecode synchronization conflict
938	Too many undefined values [%.4X]
Command Packet Error (Codes 1000-1199)	
1000	Cmd buffer overflow. keystroke lost
1002	Cmd %k is not applicable in this situation
1006	Cmd %k not implemented
1008	Cmd %k unknown
1010	Menu %d illegal
1012	Menu stack array overflow – Index %d
1014	Menu stack array underflow – Index %d
1016	No function for this command %k
ILC Error (Codes 1200-1299)	
1200	Communications processor busy
1201	Bad channel number: %d
1202	Check sum error on channel %d
1203	Bad function call: %d

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
	ILC Error (Codes 1200-1299) [Continued]
1204	Invalid message on channel %d
1205	Invalid response on channel %d
1206	No response on channel %d
1207	Channel %d not configured
1208	Communications time-out on channel %d
1209	UART error on channel %d [%.4X]
	Assembly Error (Codes 1300-1399)
1300	Auto-Assembly Can't Continue
1302	Auto-Assembly Can't Pause
1304	Auto-Assembly Can't Skip
1306	Src %i doesn't support channels m
1308	None Auto-Assembly Selected
1310	No cassette eject cmd for transport
1312	No channels selected in edit
1314	No edits selected for assembly
1316	Too many retries
1318	Task Buffer Overflow
1320	Undefined Timeline In
1322	Internal error. Unknown Auto-Assembly Command %d
1324	Internal error. Unknown Device Type
1326	Internal error. Unknown Source Request %d
1328	Internal error. Unknown transport communications %d
1330	Cannot assemble edit unless all channels (V12) are selected
1332	Assemble edits must have matching in and out points
	Trigger Error (Codes 1400-1499)
1400	GPI channel %d doesn't exist
1402	No trigger on current line

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
Character Buffer Error (Codes 1500-1549)	
1500	Cursor at start of %s buffer
1502	Cursor at end of %s buffer
1504	%s buffer closed
1505	%s buffer line done
1506	%s buffer overflow
1508	%s buffer init. with %d bytes, max is %d
1510	%s buffer underflow
Lexical Analysis Error (Codes 1550-1569)	
1550	Invalid timecode
1552	Lexcical analysis reached end of buffer
1554	Please enter value into keypad buffer
1556	Lexical analysis buffer overflow
1558	Unknown token in keypad buffer
Keypad Input Error (Codes 1570-1599)	
1570	Ascii keyboard not active here
1574	Invalid timecode in keypad buffer
1576	Cannot trim value
1578	Please enter number into keypad buffer
1580	Please enter timecode into keypad buffer
1582	No value to load into keypad buffer
1584	Number out of valid range (0 - 1000)
Task List Error (Codes 1600-1699)	
1600	Bad pDevice: %1P
1602	Invalid device action %d
1604	Invalid switcher request state %d

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
	Task List Error (Codes 1600-1699) [Continued]
1606	Invalid transport request state %d
1608	Keyboard not ready
1610	LnFieldNew %.81X overflow %.81X
1612	LnField0 %.81X wraps beyond %.81X piece
1614	LnField1 %.81X and LnFieldNew %.81X not in same piece
1616	No devices available to do request
1618	Task doesn't care if it's done
1620	Task done
1622	Task list doing clean out
1624	Task list finished execution
1626	Task list killed
1628	Task list missing
1630	Task not done
1632	Task pointer is null
1634	Task pointer %1P not found
1636	Task returned ERC_OK
1638	Task list bad
1640	Task list submit cancelled
1642	Task list has been freed [%1P]
1644	Task list already being killed
1646	Unable to do request: Device(s) not ready
1648	Task list pointer is null
1650	Task list performed twice [%1P]
1652	Unknown device type %d
	Knob Error (Codes 1700-1749)
1700	Comments Keyboard failed diagnostic test
1702	Invalid cmd sent to ACE 25 Keyboard
1704	RAM Test Failed on ACE 25 Keyboard
1706	Invalid ROM on ACE 25 Keyboard

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
Knob Error (Codes 1700-1749)	
1708	Key stuck (or held down) on ACE 25 Keyboard
1712	Knob control of %s not implemented
1714	Knob msg buffer too small
1716	Can't control EQ for %s
1718	Can't control INPUT for SRC R
File Input Error (Codes 1750-1799)	
1750	Bad config option: %s
1754	Audio channel %d not supported
1756	Unrecognized Edit line made into Comment
1760	Incomplete EDL file
1764	Found new edit during file I/O
1766	Found new line during file I/O
1768	Partial edit line during EDL file input
1770	I/O in progress. Try again, once I/O is finished
Memory Allocator Error (Codes 1800-1999)	
1800	Memory clobber type %d
1802	Bad memory region header at %1P
1804	Bad memory region: %4.4X
1806	Out of memory (memory fragmented)
1808	Out of memory (memory full)
1810	MemInitRegion: %d %1P %1P
1812	Memory test failed at %1P
EDL Error (Codes 2000-2999)	
2000	Can't turn off all channels
2002	Sorry, cannot change src speed with zero duration times

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
	EDL Error (Codes 2000-2999) [Continued]
2004	Sorry, source times stay at zero duration duration on zero speed transport
2006	Can't clean against an undefined entry on edit %1d %c
2008	Current line is not a key effect line
2010	Can't do an ALL %k
2012	Can't %s on Record machine or Static source
2016	Can't split edit line
2018	Can't tag EDL edit
2020	Can't change/clear static source entry time
2022	Can't change to undefined trigger time
2024	Source has mismatched fields
2026	Source %i not color framed
2028	Source %i not pal paired
2032	Change cancelled
2034	Edit change not supported on %s line
2036	Edit change request not valid %.4X
2038	No mode given
2040	No edit source specified
2042	No record entry time given
2044	No record times given
2046	No source entry time given for %i
2048	No source times given for %i
2050	No trigger time given
2052	Record Entry greater than Exit
2054	Speed must be between -100 and 300
2056	Undefined source speed
2058	CMX I/O - Edit numbers out of range (001-999). Please renumber EDL.
2059	Reel %i out of range. Please renumber. Valid range is 1-253.
2060	Too many different reel numbers in CMX list
2061	CMX I/O: too many sources. Please write list in pieces.
2062	Key background has delay

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
	EDL Error (Codes 2000-2999) [Continued]
2064	Duration and speed are in conflicting directions
2066	Different edits
2068	Edit needs to be divided
2070	Edit has no edit line
2072	Edit size %1P %d is too large
2074	Effect change not supported on %s line
2076	Effect cannot change from %s to %s
2077	Effect duration too high
2078	Effect End outside of legal range
2084	User has not marked a first edit
2086	User has not marked a last edit
2088	No FROM line found
2090	Found no match
2092	No TO line found
2098	Gpi %i is not known by system
2102	Cannot delete last edit line
2104	Bad line border type %.4X
2106	Bad line pointer %1P
2108	Bad line type %1P %.4X
2110	List is empty
2112	Reached end of list
2114	Reached start of list
2116	Cannot enter negative effect duration
2118	Cannot make record duration less than zero
2120	Nothing to Undo
2122	Key background has no delay
2126	No machine src %i in edit. Cannot change to Src Abs Trigger
2128	No timecode in current edit line
2130	Cannot mark. Source %i is not a transport
2132	Cannot assign an edit number of zero

(Continued next page)

Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
	EDL Error (Codes 2000-2999) [Continued]
2134	Open ended edit
2136	Undefined duration
2138	Query type: %.4X, Source: %i, Channel(s): %.4X not found
2124	GPI is not here
2140	Query not supported on %s line
2144	Undefined record entry
2146	Undefined record exit
2148	Record times have gaps
2150	Record times overlap
2152	Reel %s not found
2154	Undefined reel
2158	Cannot sort (internal failure)
2160	Edit split into %d channel combinations
2164	Source %i not found
2166	Source speed not constant
2168	Source times not synchronous
2170	Bad data in viewport
2172	Source is static
2174	Tag not supported on %s line
2174	SYNC TAG failed
2178	REEL TAG failed to find previous use of current source %i in EDL
2182	Trigger src %i does not match current source
2186	gfProtectUndo TRUE
2188	Invalid pattern value
	Transport Error (Codes 3000-3999)
3000	Cannot control source: %i
3002	No color framing with component reference
3004	Invalid source selected: %d
3006	Illegal slow motion speed: %d

(Continued next page)

Table A-2. ACE 25 Error Messages (Continud)

Code No.	Error Message or Meaning
	Transport Error (Codes 3000-3999) [Continued]
3008	No edit to replay
3010	Transport %c stopped at end of tape
3012	Can't search for undefined timecode
3014	Sony Communications Error: %4.4X
3016	Sony sync distance: [%81d] [%81d]
3018	Unknown Src Ctrl Cmd %d
3020	Source %i needs longer preroll time
3022	Source %d is unmounted
3024	Unknown timecode source on Transport %d
3026	Transport can't do switcher action %s
3028	Transport can't do %s during %s
3030	Transport %c can't load its tape time
3032	Transport %c not cued
3034	Transport %c not ready
3036	Transport %c not synchronized
3038	Transport Status: %s Transport %c not synchronized
3040	Transport %c never synchronized
	Switcher Error (Codes 4000-4999)
4000	Switcher can't do %s during %s
4002	Switcher can't do transport action %s
4004	Can't control effect %s on %s
4006	Can't control fader for effect %s
4008	Can't control key for effect %s
4010	Can't handle request %s on %s
4012	Can't control width for effect %s
4014	Can't find effect data for this effect
4016	Can't control effect WIPE, must use external switcher, e.g. VISTA
4018	%s switcher can't control audio 1 & 2 separately

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Table A-2. ACE 25 Error Messages (Continued)

Code No.	Error Message or Meaning
Switcher Error (Codes 4000-4999) [Continued]	
4020	Dumpster Memory Failure: Addr .2X, Wrote %.2X, Read %.2X
4021	Internal switcher not capable of more than 4db gain
4024	Invalid metering point: (%.4X)
4026	Invalid metering type: (%.2X)
4028	Timeout waiting for line count %d
4030	Switcher needs longer preroll for effect %s
4032	This switcher supports no AUDIO
4034	This switcher supports no effects
4036	No need to build tasks for current line
4038	%s switcher supports no VIDEO
4040	%s switcher not ready
4042	Pattern number %d too big
4044	Pline bad in switcher request
4046	Invalid switcher request %d
4048	Switcher request %s not supported
4050	Switcher type %d not supported
Unallocated/Special (Codes 5000-9999)	

Note: The characters X or % are replaced by characters or digits in actual displayed messages.

APPENDIX B

TELEVISION STANDARD CONVERSIONS

B-1 INTRODUCTION

The ACE 25 system operates in one of three television standards:

- NTSC
- PAL
- PAL-M

Jumpers on the Color Field 1 ID PWA and the Video Timing PWA select the appropriate television standard. Voltage settings for the Edit Controller unit, keyboard, and monitor must match the supply voltages, but do not affect the television standard.

B-2 COLOR FIELD 1 ID PWA

Table B-1 shows the jumper settings for the Color Field 1 ID PWA. Refer to Figure 8-1 for the location of these jumpers.

B-3 VIDEO TIMING PWA

Table B-2 shows the jumper settings for the Video Timing PWA. Refer to Figure 9-1 for the location of these jumpers.

B-4 VOLTAGE SELECTION

The ACE 25 system operates from power that supplies either of two voltage ranges: 90-132 Vac or 180-264 Vac, with a 50 or 60 Hz line frequency, single phase. The Edit Controller unit, keyboard, and data monitor must match the voltage range of the power supply. Voltage changeover procedures for the Edit Controller unit are covered in paragraph 5-7, for the keyboard in paragraph 16-4 , and for the monitor in paragraph 16-10 .

Table B-1. Color Field 1 ID PWA Jumper Selection

Jumper	NTSC	PAL	PAL-M
J7	NTSC	Opposite NTSC	Opposite NTSC
J9	525	625	525

Table B-2. Video Timing PWA Jumper Selection

Jumper	NTSC	PAL	PAL-M
J5	525	625	525
J6	NTSC	PAL	PAL
J7	525	625	525

APPENDIX C

VPR-2/VPR-2B MODIFICATION

C-1 INTRODUCTION

The Ampex VPR-2 and VPR-2B require a modification in order to be used with the ACE editing systems, such as the ACE 25, and a MIF (Machine Interface) unit to convert serial communications from the editor to parallel communications for the VTR.

Note

The MIF unit can be mounted inside the VPR-2 console using optional kit P/N 1430626.

To interface the VPR-2 or VPR-2B VTR with an ACE system, the following items must be completed:

- Installation of the Modification Kit for VTR (P/N 1430538)
- Installation of boot ROM in MIF unit version P/N 1431302-02 or later
- Setting of DIP Switch S2 on MIF Personality PWA correctly (see paragraph C-2)
- Adjustment of R24 on Capstan Servo PWA in VTR (see paragraph C-3)

The Modification Kit contains installation directions, and affects the following PWAs in the VPR-2 or VPR-2B VTR:

- Audio PWAs 1400020, 1400026
- Capstan Servo PWAs 1400150, 1400153
- Control PWAs 1400170, 1400173, 1400176
- Search PWAs 1400180, 1400183
- Motherboard PWA 1400426

C-2 DIP SWITCH S2 SETTING

DIP Switch S2 on the MIF Personality PWA is set for the VPR-2 and VPR-2B as shown in Table C-1:

Table C-1. DIP Switch S2 Setting on MIF Personality PWA

VPR-2	VPR-2B
Position 1: CLOSED	Position 1: OPEN
Position 2: CLOSED	Position 2: CLOSED
Position 3: CLOSED	Position 3: CLOSED

C-3 R24 ADJUSTMENT ON CAPSTAN SERVO PWA

The adjustment procedure for R24 on the Capstan Servo PWA requires an Extender PWA and an oscilloscope. The following procedure is used to make this adjustment:

1. Turn off VTR power.
2. Remove Capstan Servo PWA and place on Extender PWA.
3. Connect oscilloscope to TP4 on Extender PWA.
4. Set REMOTE/LOCAL switch to LOCAL position.
5. Load tape reel and power on VTR.
6. Press SLOW switch on VTR and set speed control to maximum clockwise position.
7. Adjust R24 on Capstan Servo PWA to produce a waveform at TP4 with a minimum period of 350 microseconds. VTR reels should not oscillate.
8. Turn off VTR power.
9. Remove Capstan Servo PWA from Extender PWA, and replace in VTR.

APPENDIX D

INTERNAL SWITCHER INSTALLATION

D-1 INTRODUCTION

Internal audio and video switchers can be installed in ACE 25 units after delivery. The installation procedure may involve some or all of the following procedures:

- Switcher Backplane Assembly Installation
- Dumpster Bus Interface PWA Installation
- Audio Switcher PWA Installation
- Video Timing PWA Installation
- Video Switcher PWA Installation
- Final Detail

D-2 SWITCHER BACKPLANE ASSEMBLY INSTALLATION

To install the Switcher Backplane Assembly:

1. Power off equipment.
2. Disconnect all cables to ACE 25 Edit Controller Chassis.
3. Remove Edit Controller unit from mounting and place on flat surface.
4. Remove top cover of Edit Controller.
5. Remove blank lower rear panel of Edit Controller chassis, which is secured by 12 cross-recessed screws.
6. Unpack Switcher Backplane Assembly. The flat ribbon cable should be connected at this time (note position of key in connector). The five-pin connector is attached to the J4 connector on the Switcher Backplane Assembly. This cable should be wrapped around the side of the assembly between the PWA and the mounting base.
7. Feed two cables from Switcher Backplane Assembly through slot inside chassis.

8. Attach Switcher Backplane Assembly to Edit Controller chassis using screws for blank lower rear panel.

Note

Do not tighten screws until all screws are inserted and assembly is positioned correctly.

D-3 DUMPSTER BUS INTERFACE PWA INSTALLATION

To install the Dumpster Bus Interface PWA:

1. Perform steps 1 through 4 in paragraph D-2, to remove the Edit Controller unit cover.
2. Unpack Dumpster Bus Interface PWA.
3. Attach flat ribbon cable to Dumpster Bus Interface PWA (note position of key in connector).
4. Remove two cross-recessed screws securing bar holding PWAs in place.

Note

These screws may be difficult to remove.

5. Insert Dumpster Bus Interface PWA into slot 7 in CPU Motherboard PWA.

D-4 AUDIO SWITCHER PWA INSTALLATION

To install the Audio Switcher PWA:

1. Unpack Audio Switcher PWA.
2. Lower front cover of Edit Controller chassis.
3. Carefully slide Audio Switcher PWA into upper slot along bottom front of the Edit Controller chassis.
4. Firmly seat Audio Switcher PWA in rear connectors, using side levers on PWA.
5. Close front cover of Edit Controller chassis.

D-5 VIDEO TIMING PWA INSTALLATION

If a video switcher is installed, a Video Timing PWA must also be installed. The Composite Video Timing PWA will work with both versions (Component and Composite) of the internal video switcher. The Component Video Timing PWA will work only with the Component internal video switcher.

To install the Video Timing PWA:

1. Unpack Video Timing PWA.

2. Connect coax ribbon cable (P/N 1430931) supplied with PWA to connector on Video Timing PWA.

Note

Large key in connector faces away from PWA.

3. Connect one end of six-inch BNC-Coax-BNC cable to BNC connector on Video Timing PWA.

4. Install Video Timing PWA in slot 6 of CPU Motherboard PWA in Edit Controller chassis.

5. Attach other end of coax ribbon cable to connector on top edge of Dumpster Bus Interface PWA.

6. Attach other end of six-inch BNC cable to open BNC connector on Color Field 1 Detector PWA (also known as the Color Framer PWA).

7. Carefully install multi-coax cable into connection on Switcher Backplane Assembly. Press connector firmly down to secure cable in place.

Note

Large key faces front of ACE 25.

D-6 VIDEO SWITCHER PWA INSTALLATION

To install the Video Switcher PWA:

1. Unpack Video Switcher PWA.

2. Lower front cover of Edit Controller chassis.

3. Carefully slid Video Switcher PWA into the lower slot located along the bottom front of the Edit Controller chassis.

4. Firmly seat Video Switcher PWA in the rear connectors, using side levers on PWA.

5. Close front cover of Edit Controller chassis.

D-7 FINAL DETAIL

After all PWAs have been installed:

1. Check all cable connections and ensure all PWAs are firmly set in slots.
2. Replace support bracket securing PWAs into CPU Motherboard PWA slots.
3. Replace top cover of Edit Controller chassis.
4. Replace cables connected to rear panel of Edit Controller chassis.

For information on operation of the Audio Switcher and Video Switcher, refer to the *ACE 25 Operation* Manual.